SOLDER BUMP FLIP CHIP BONDING FOR PIXEL DETECTOR HYBRIDIZATION

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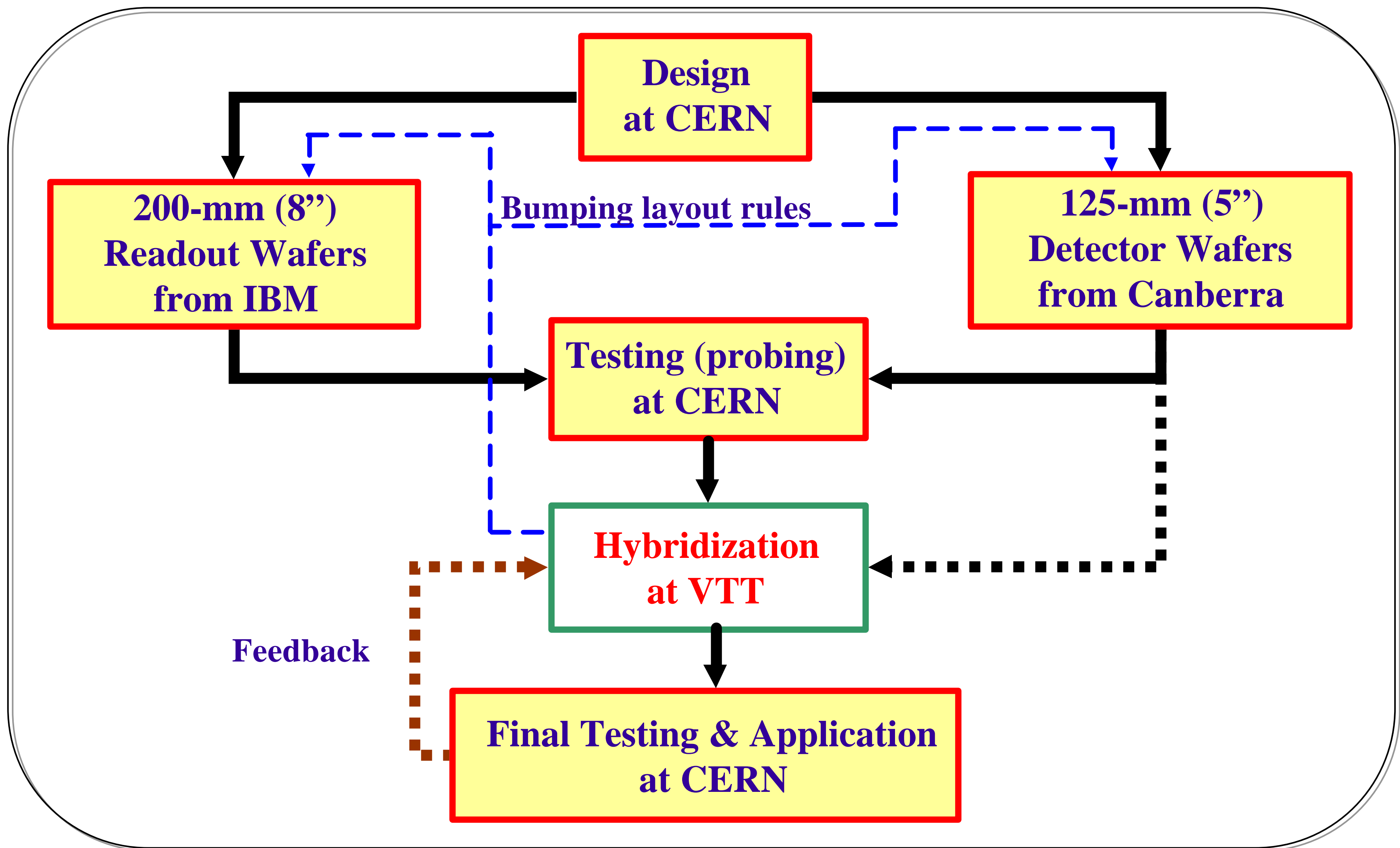
Outline

- Logistics
- Bumping Process
- Facilities/Equipment
- Thinning of Wafers
- Flip Chip Assembly
- Application Example: CERN ALICE Assembly
- Yield Factors
- Shortlist of Things
- Future Trends
- Summary

Logistics



VTT

Process Steps for Hybridization at VTT

- Solder Bumping of Readout Wafers
- Solderable Pads on Detector Wafers

← Done in Class-10 clean room

- Optional Thinning of (Readout) Wafers

- Dicing

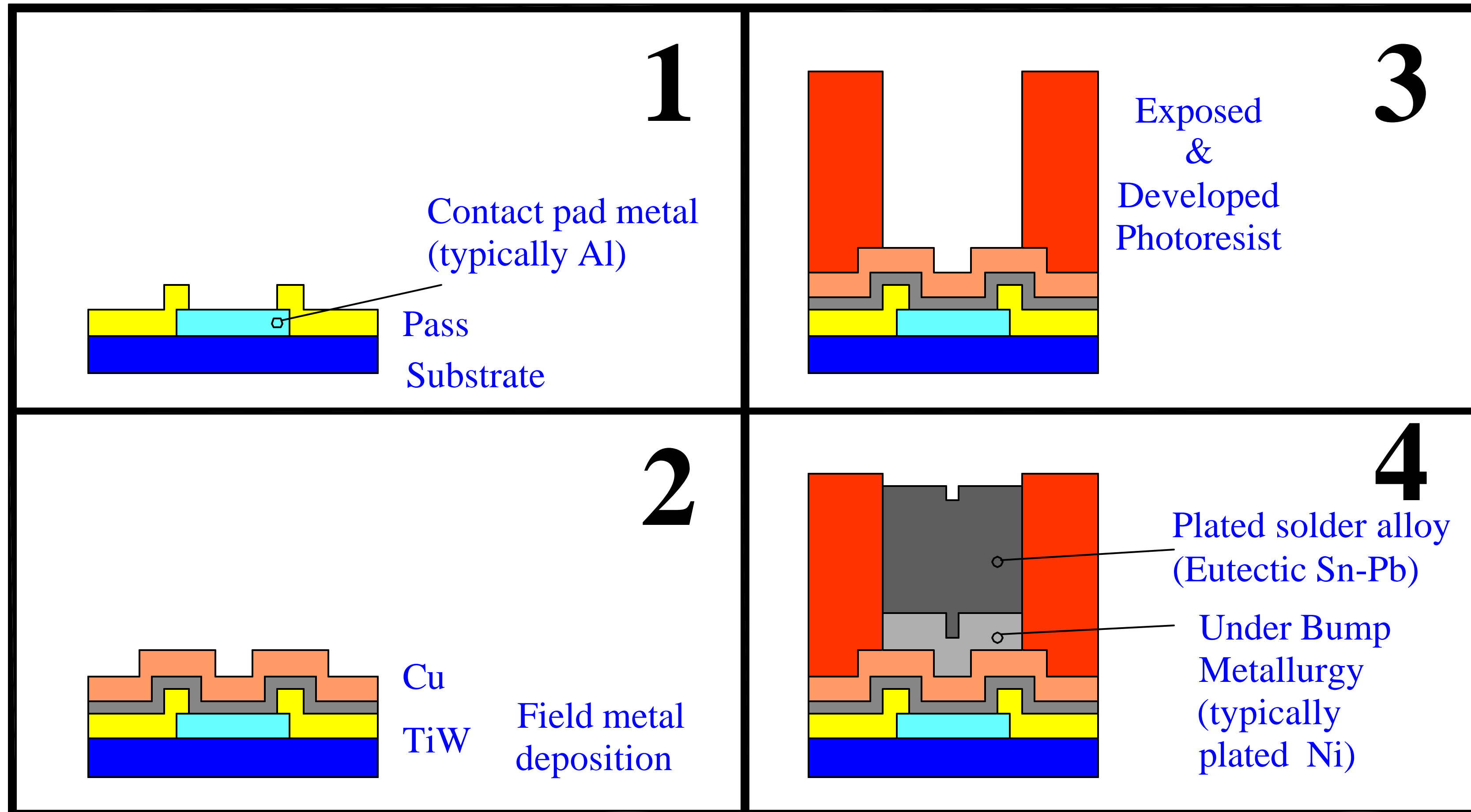
- Flip Chip Bonding

← Done in Class-10 clean room

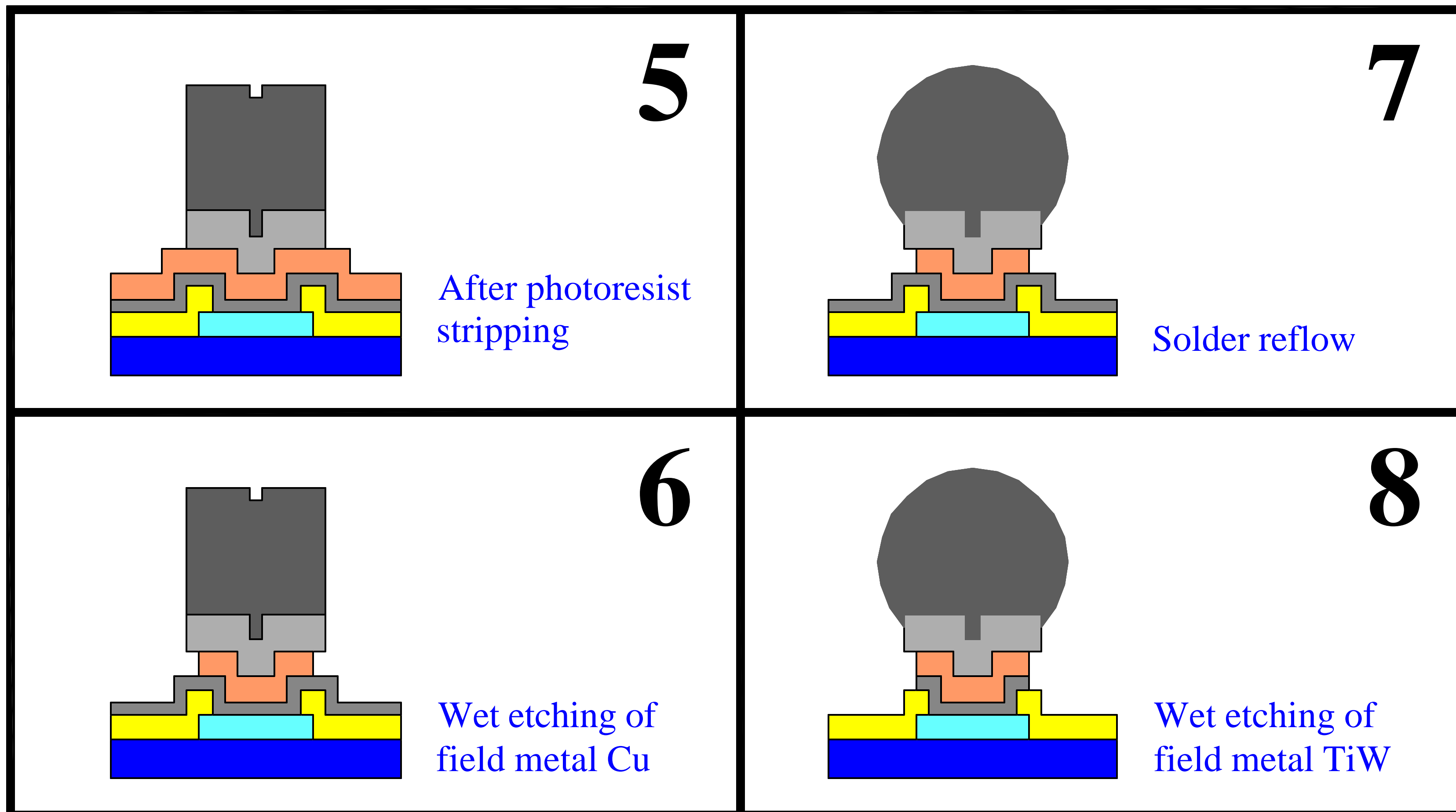
Flip Chip Process: Key Features

- **200-mm (8”) wafer capability.**
- **Tin-lead solder alloy bumps are used for mechanical strength of bonded assemblies.**
- **Bump deposition by electroplating.**
- **Process is compatible with wire bonding pads and unpassivated backside metallization.**
- **Thinning (back grinding) of bumped readout wafers.**
- **‘Clean’ dicing with front side protection using either photoresist or tape.**
- **Fluxless flip chip bonding.**

Bumping Process



Bumping Process [cont'd]

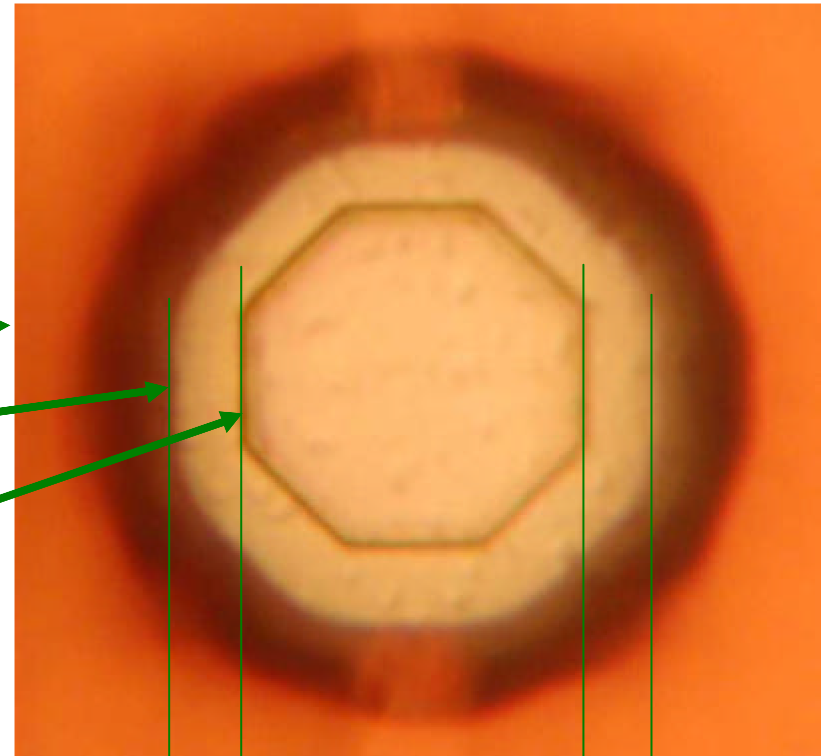


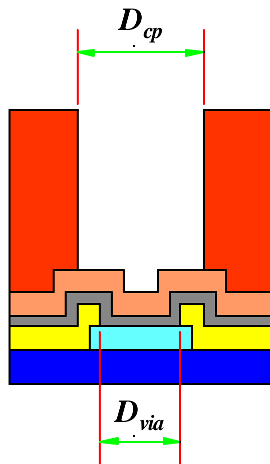
Processes/Equipment at VTT

PROCESS	EQUIPMENT
Photoresist coating	Suss MicroTec ACS200
Mask Aligners	Suss MicroTec MA6 & MA200CC
Thin film sputtering	Von Ardenne CS730S, MRC 903
Electroplating (Ni, Sn-Pb)	Proprietary System
Bump Reflow	ATV SRO-704-R formic acid oven
Wafer Thinning	Strasbaugh 7AF Intelligent Grinder
Dicing Saw	Disco DFD651
Flip Chip Bonder	Suss MicroTec FC150

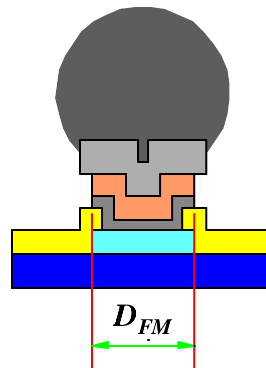
Photolithography Step for Bumping

Bump opening on mask overlaps passivation via. Overlap is determined by field metal underetching & alignment accuracy.





passivation via



final bump foot

Example: CERN ALICE1/LHCb readout.

Wafer Thinning

Thinning is preferably done after bumping!

PROCESS STEPS

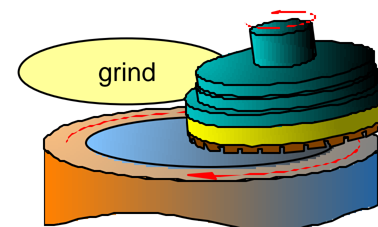
① Front side protection/planarization: UV-curable back grinding tape laminated on bumped wafer.

② Back grinding using diamond wheels with two different grit sizes (coarse + fine).

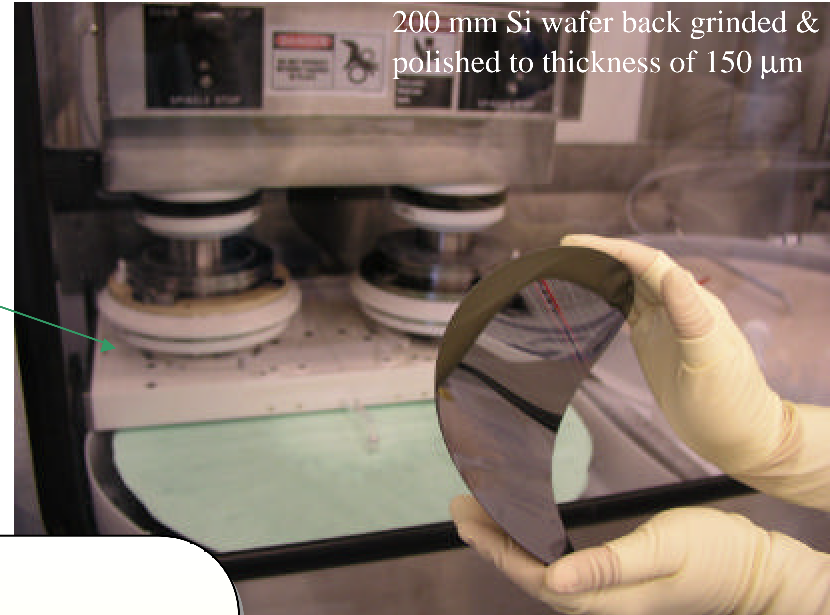
③ Defect layer left by mechanical grinding is removed by wet chemical etching or CMP (Chemical Mechanical Polishing).

④ Protective tape is UV-exposed and delaminated.

Strasbaugh 7AF Intelligent Grinder



Wafer Thinning [cont'd]



Strasbaugh 6DS-SP CMP System

NOTES

- **Thickness down to 150 mm (200-mm/8" wafers).**
- **Total thickness variation (TTV) with protective tape < 5 mm over wafer.**
- **Post-grinding defect layer etching improves mechanical strength of die.**

Flip Chip Bonding

Flip chip assembly is done in a Class-10 clean room.

Suss MicroTec FC150 Flip Chip Bonder with both Universal and Solder Reflow Bonding Arms.

PROCESS STEPS

① **Preliminary alignment.**

② **Detector and readout chips are adjusted exactly parallel using a laser autocollimator.**

③ **Lateral alignment (x,y, q).**

④ **Pre-bonding compression of softened bumps.**

⑤ **Reflow bonding.**

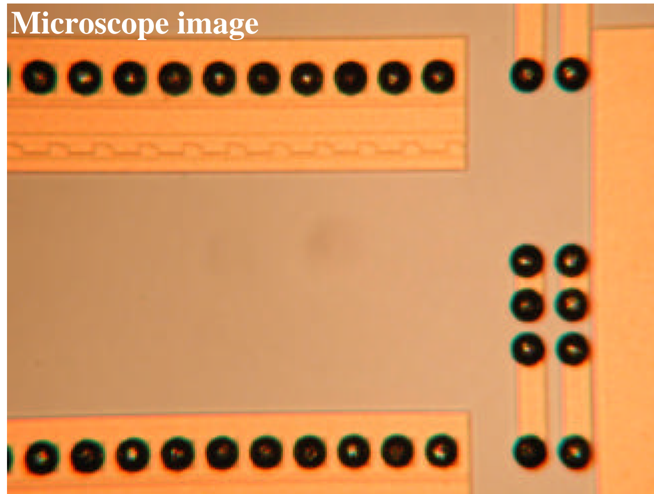
⑥ **Cooling.**

NOTES

- **Chips are heated through custom SiC vacuum tools using infrared halogen lamps.**
- **Alignment accuracy: < 3 mm.**
- **Throughput: 3-4 bondings/hour.**

Example: ALICE 'Ladder' Assembly

1. Readout



ALICE1/LHCb readout chip process

- **Readout wafer size 200 mm x 725 μm**
- **Bumping with eutectic solder: TiW/Cu/Ni(3 μm)/eut. Sn-Pb(13 μm)**
- **Bump pitch: x = 50 μm / y = 400 μm**
- **Wafer thinning to 150 μm**
- **Dicing to chip size of 13.7 mm x 15.9 mm**
- **Picking of KGD**
- **Number of bumps/chip: 8,192**

Solder Bump on ALICE1/LHCb Readout Chip After Reflow

Target Solder Volume = 1.52×10^{-14} m^3

Eutectic Sn-Pb solder alloy

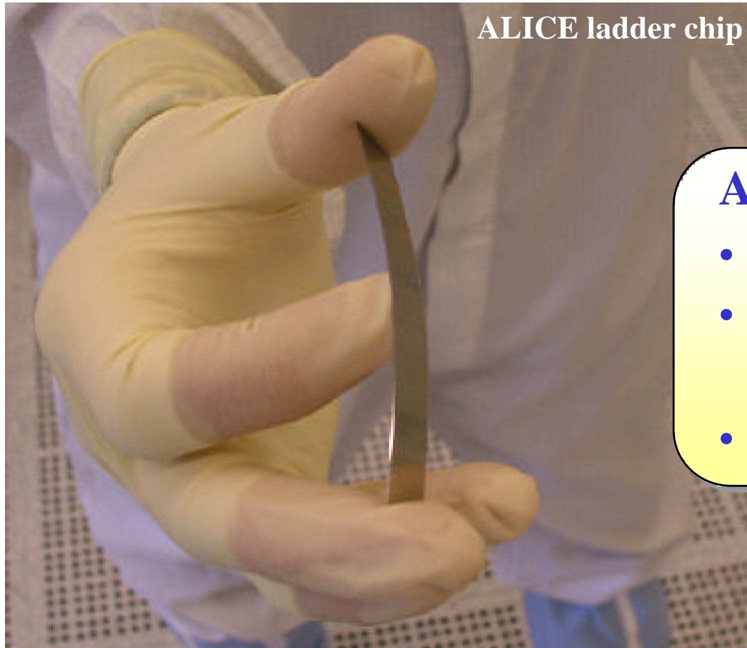
Ni

TiW/Cu

Mag = 6.04 K X
WD = 3 mm
2µm*
EHT = 20.00 kV
Detector = InLens
Store resolution = 1024 * 768
Date :2 Nov 2001 Time :14:08:22
VTT Microelectronics Centre

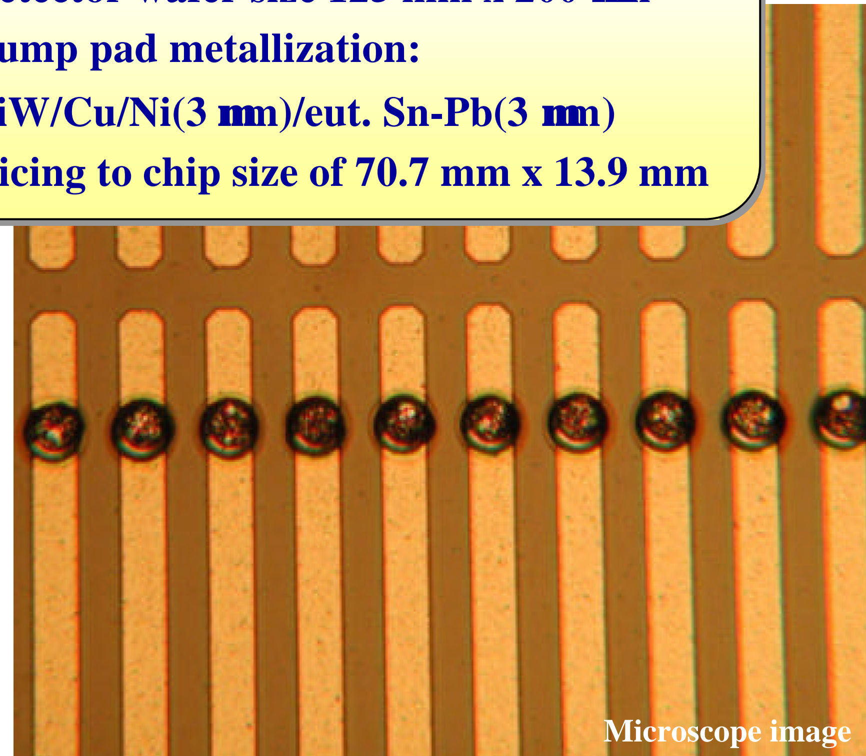
ALICE 'Ladder' Assembly [cont'd]

2. Detector



ALICE detector chip process

- **Detector wafer size 125 mm x 200 mm**
- **Bump pad metallization:**
  TiW/Cu/Ni(3 mm)/eut. Sn-Pb(3 mm)
- **Dicing to chip size of 70.7 mm x 13.9 mm**

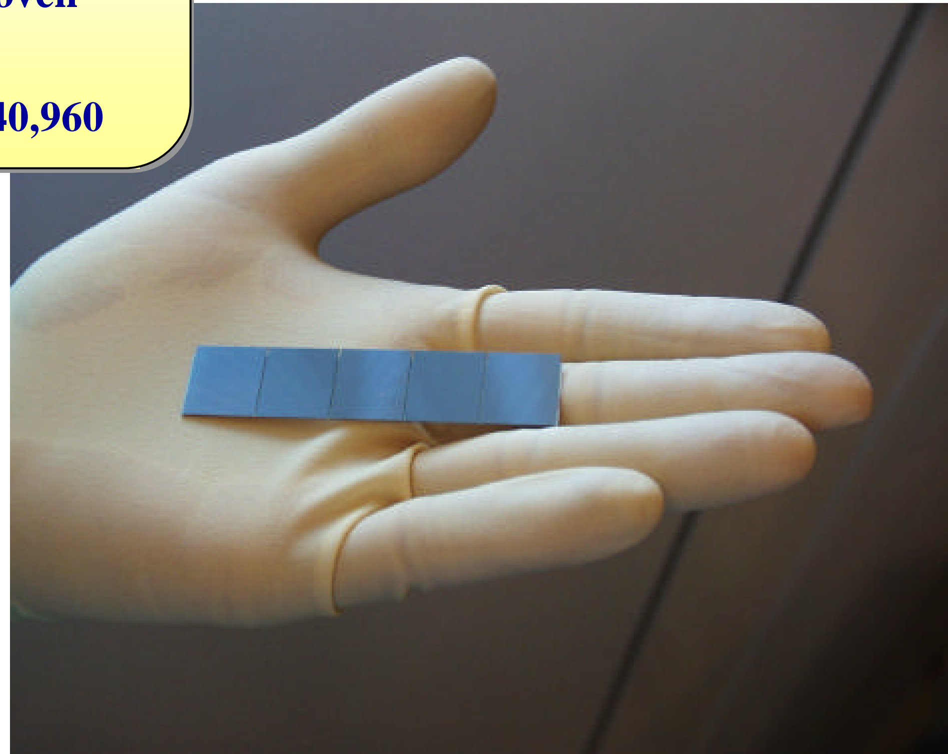


ALICE 'Ladder' Assembly [cont'd]

3. Flip chip bonding

Hybridized ALICE assembly

- **Five ALICE1/LHCb readout chips flip chip bonded on ALICE1 detector ladder chip**
- **Assembly reflow using formic acid oven**
- **Chip-to-substrate distance: 20 mm**
- **Total number of bumps/assembly: 40,960**

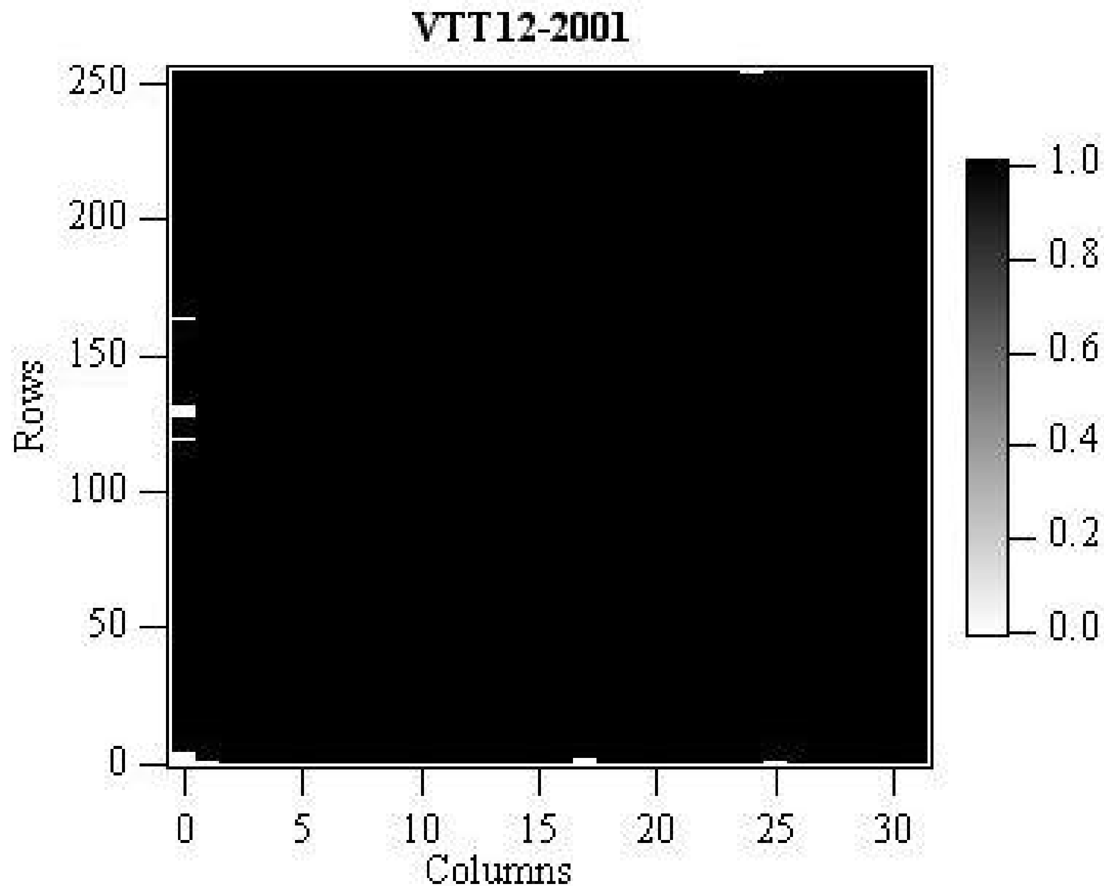


Process Customization

- **VTT's 'generic' flip chip process has been customized to the wafers used by CERN, with consequent improvements in yield.**
  - **Field metal deposition on detector side: compatibility with polyimide passivation used.**
  - **Protection of detector wafer backside for bumping process.**
  - **Field metal etching: both sides.**
  - **Reflow on readout side.**
  - **Detector dicing process.**
  - **Flip chip bonding parameters.**
  - **10-90 Sn-Pb solder process for LHCb assembly.**

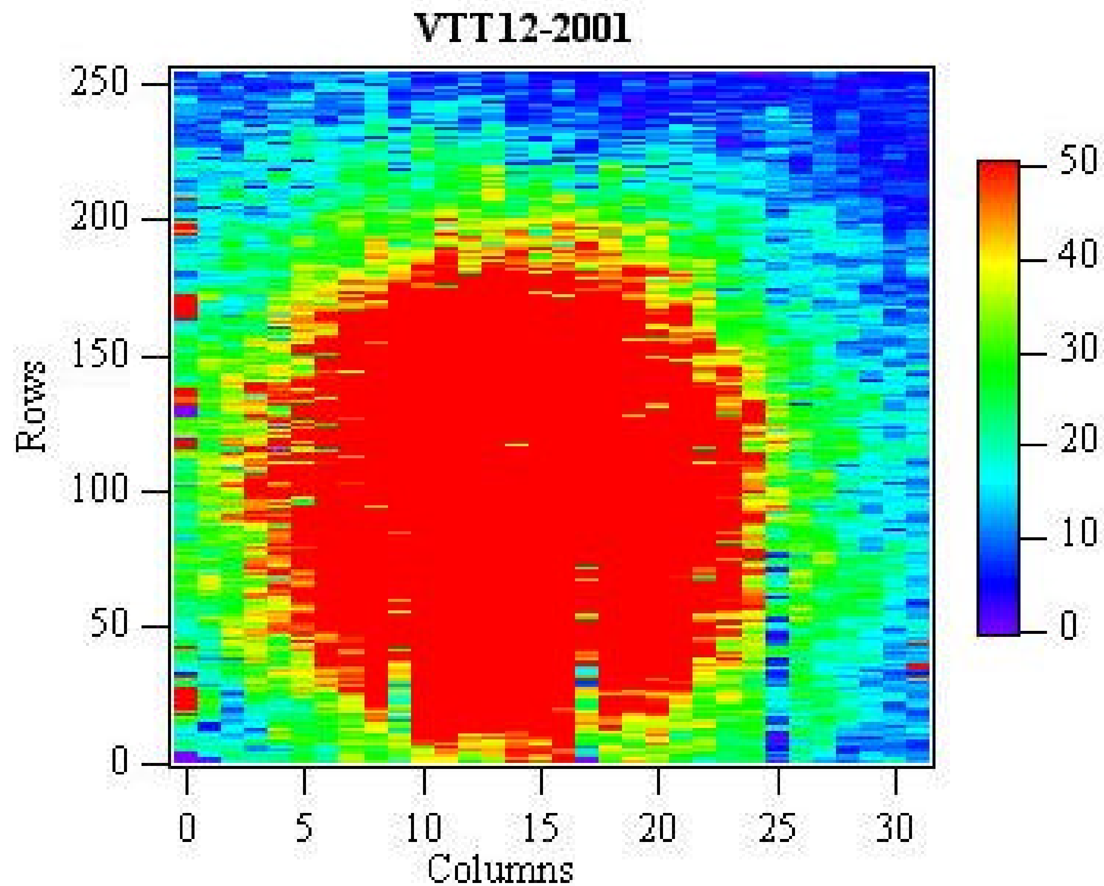
ALICE1 Single: “VTT12”

“VTT12” assembly (an early one, made in 2001) irradiated with a strontium source. Output scaled to “1” to show dead pixels. The number of dead pixels is 14 out of a total of 8,192.



ALICE1 Single: "VTT12"

"VTT12" assembly irradiated with a strontium source. Output scaled to max. "50" to show intensity of beam. The columnar imperfections are due to artefacts of the readout chip.



Yield Factors

- **Pre-bumping/assembly.** Foundry yield, particles generated in probing and handling (and history of wafers in general). Detector side: Defects in polyimide passivation.
- **Bumping/assembly.** Missing bumps, shorted bumps, high contact resistance (influenced by history of wafers), detector dicing, bonding yield.
- **Post-bumping/assembly.** Handling, correct test procedure, interpretation of test results.

Shortlist of Things...

- **Bumping layout design**
  - **Alignment targets with known locations are required on wafers (and matching targets on masks).**
  - **Three smooth areas of at least 50 mm in diameter are needed on both detector and readout chips at the same mutually aligned locations near chip periphery for laser leveling in flip chip bonder.**
  - **Preferably single dicing lane in between chips, and no metal on dicing lanes (on either side of wafer). Avoid layouts which cannot be diced in a single run. Kerf width in dicing is non-zero!**
  - **Potential stitching problem with stepper-processed wafers (1:1 contact aligners used at VTT).**

Shortlist of Things... [cont'd]

- **Readout & detector wafers**
  - **Minimize handling of wafers outside clean room environment.**
  - **Probing marks may have an effect on bumping process.**
  - **Whole wafers preferred for bumping!**

Future Trends

- Reliable flip chip bonding process with bump size of around 10 mm in diameter will be needed in near future.
- Use of non-Si detector materials gives rise to thermal mismatch in contrast to readout asic made of Si. Low melting point solder alloys needed to minimize thermal stress.
- Lead free solder bumps?
- For large area pixel detectors, bump bonding alignment and autocollimation accuracy needed is at the limit of existing tools.

VTT

Summary

- A brief overview of VTT's bumping and flip chip assembly capabilities was presented.
- The hybridization of CERN's ALICE detector was shown as an example.