LOW MASS SEMICONDUCTOR TRACKERS using THIN PIXEL DETECTORS

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Workshop Radiation Hard Semiconductor Devices for Very High Luminosity

CERN

28 - 30 November 2001

FUTURE EXPERIMENTS

1. ELECTRON or MUON COLLIDERS

2. HADRON COLLIDERS

3. HEAVY ION COLLIDERS

COMMON NEEDS

TAGGING of EVENTS

-> JETS in CALORIMETER

-> 2nd VERTICES by TRACKING

IMPROVE SELECTIVITY : NEXT ?

-> MATERIAL limits PRECISION

-> RESOLVE JETS

look for decays inside ??

FUTURE EXPERIMENTS

ELECTRON or MUON COLLIDERS

MODERATE MULTIPLICITY

< hundred per event

LOW RATE Hz - kHz

“HIGH” LUMINOSITY ??

TRACKING NEEDS (Damerell)

HIGH PRECISION ~1 µm

--> SMALL SEGMENTS

THIN DETECTORS

SIGNAL in 25 µm Si : 1500 e$^-$ ~ 5 keV

--> LOW NOISE < 60 e$^-$ rms

CRYOGE NIC OPERATION for low noise

--> IN VACUUM

CCD or CMOS IMAGERS may work

--> ms between events

“LOW” RADIATION DOSE

FUTURE EXPERIMENTS

HADRON COLLIDERS

VERY HIGH LUMINOSITY

INCREASE OF INTENSITY

DOUBLE (?) FREQUENCY

INCREASE SPEED OF TRACKER DETECTORS

CRYOGENIC OPERATION
THINNER SENSORS
FASTER SHAPING ELECTRONICS
--> MORE POWER
MORE DATA

BETTER RADIATION HARDNESS

SENSORS :
DIFFERENT APPROACHES POSSIBLE
ELECTRONICS : DEEP SUBMICRON OK ?

DECREASE MATERIAL

GENERAL NEED

THIN DETECTORS
NEED
LOW NOISE READOUT

THIN DETECTORS NEED LOW NOISE READOUT

SLOW

and/or

SMALL SEGMENTS

THIN SENSORS

HIGH LUMINOSITY IMPOSES FAST ELECTRONICS
THUS, “HIGH” POWER
different optimization for e -colliders

LOW NOISE + HIGH SPEED ACHIEVED in HYBRID PIXEL DETECTORS

REDUCE MATERIAL in TRACKER
easier for e -colliders
RADIATION TOLERANCE to
> 100 Mrad, ~10^{15} n cm^{-2}

RADIATION LENGTH PIXELS

OMEGA2 PIXELPLANE

AREA 30 cm^2

WITH OVERLAPS

Si SENSOR	0.42 %		
Si CHIPS	0.44		
BUMPS	0.004		
CERAMIC	0.88	->	0.66 %
Cu lines	0.1		
TOTAL	1.84 %		

AIR COOLING

OMEGA3 is THINNER 1.62 %

DELPHI VFT PIXELMODULE

AREA 7.3 cm^2

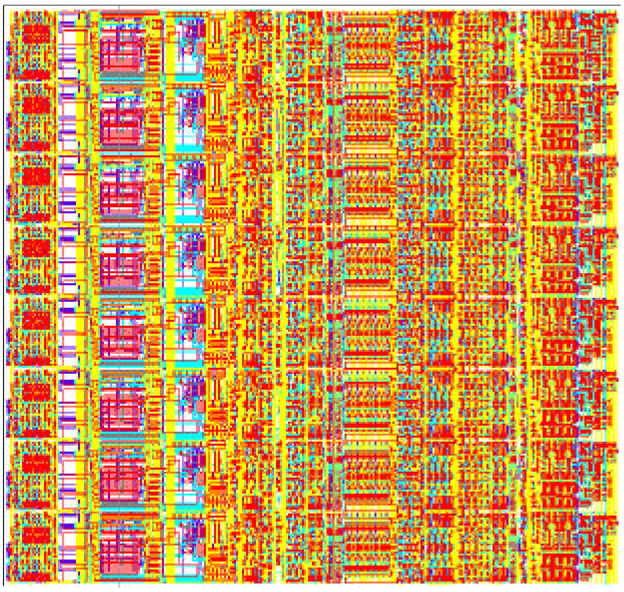
Si SENSOR, BUMPS & CHIPS	1.45 %
KAPTON, CAPACITORS	0.71
TOTAL	2.15 %

AIR COOLING

MECHANICAL SUPPORT NOT COUNTED

CURRENT PIXEL DETECTORS in PARTICLE PHYSICS

eg ALICE HEAVY-ION EXP

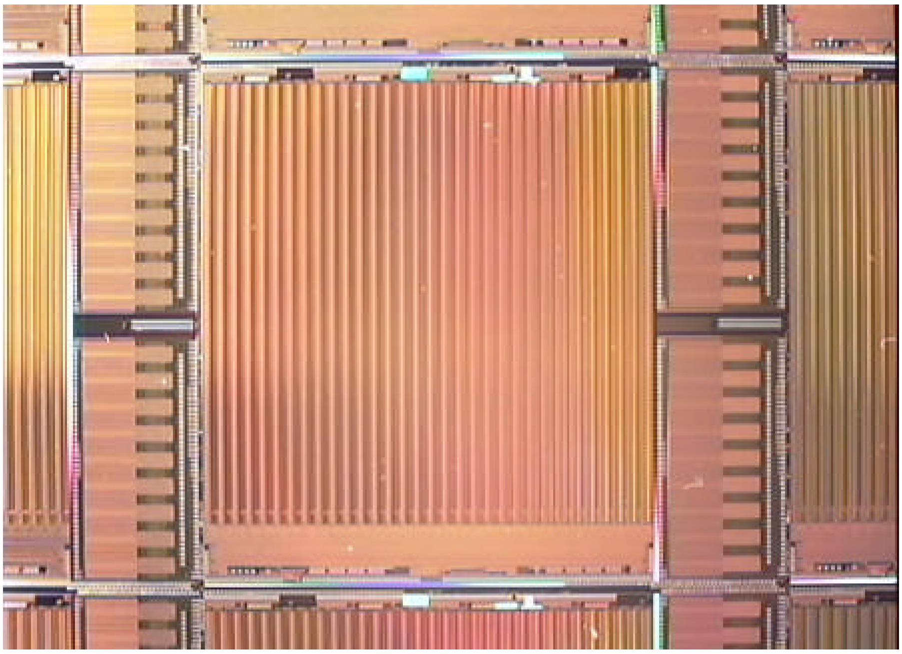


8 cells, blocked

radhard 30 Mrad

400µm x 425µm

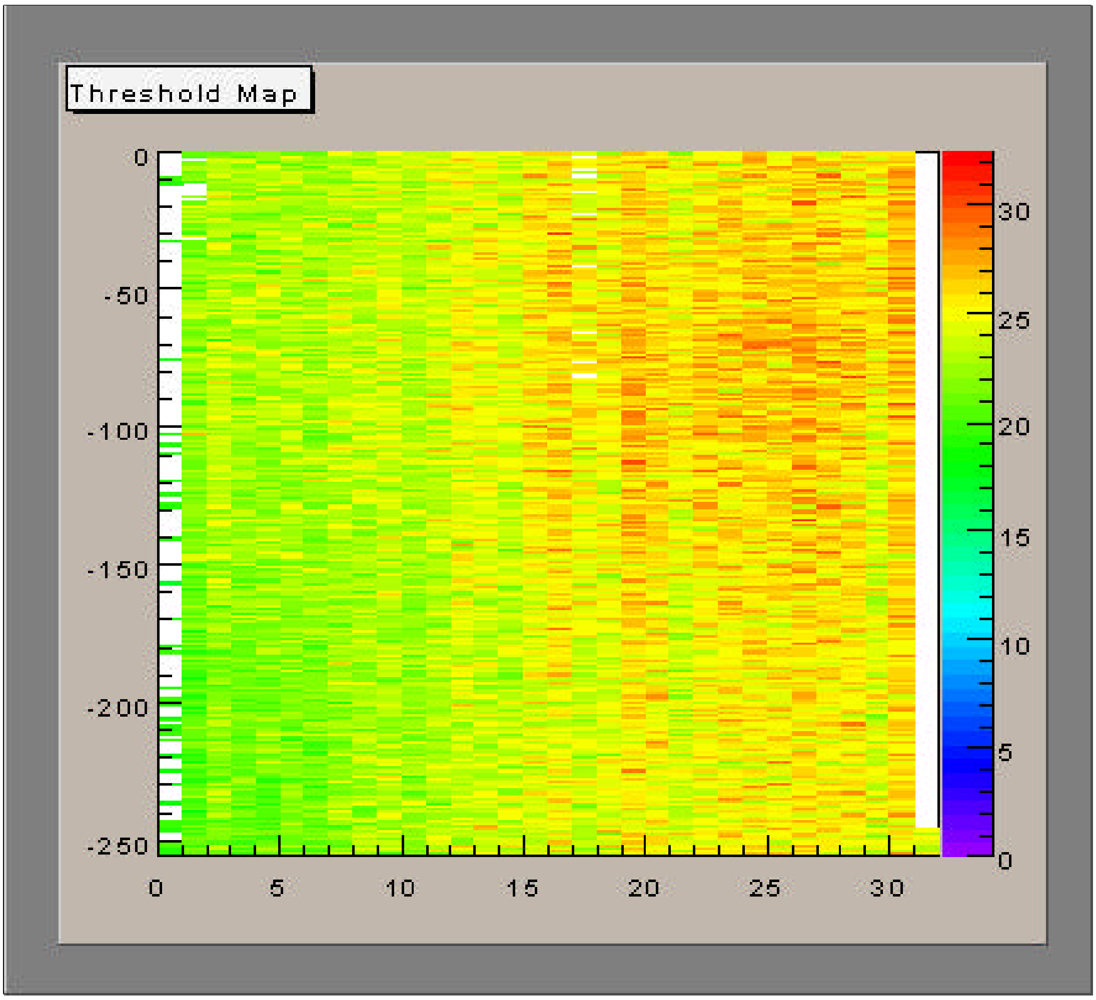
8000 pixels, 13 M transistors, 2.2 cm^2



ALICE PIXEL DETECTOR

PRELIMINARY, CHIP ONLY

8000 pixels, threshold distribution



threshold ~25 mV = 800 e^-

UNCALIBRATED

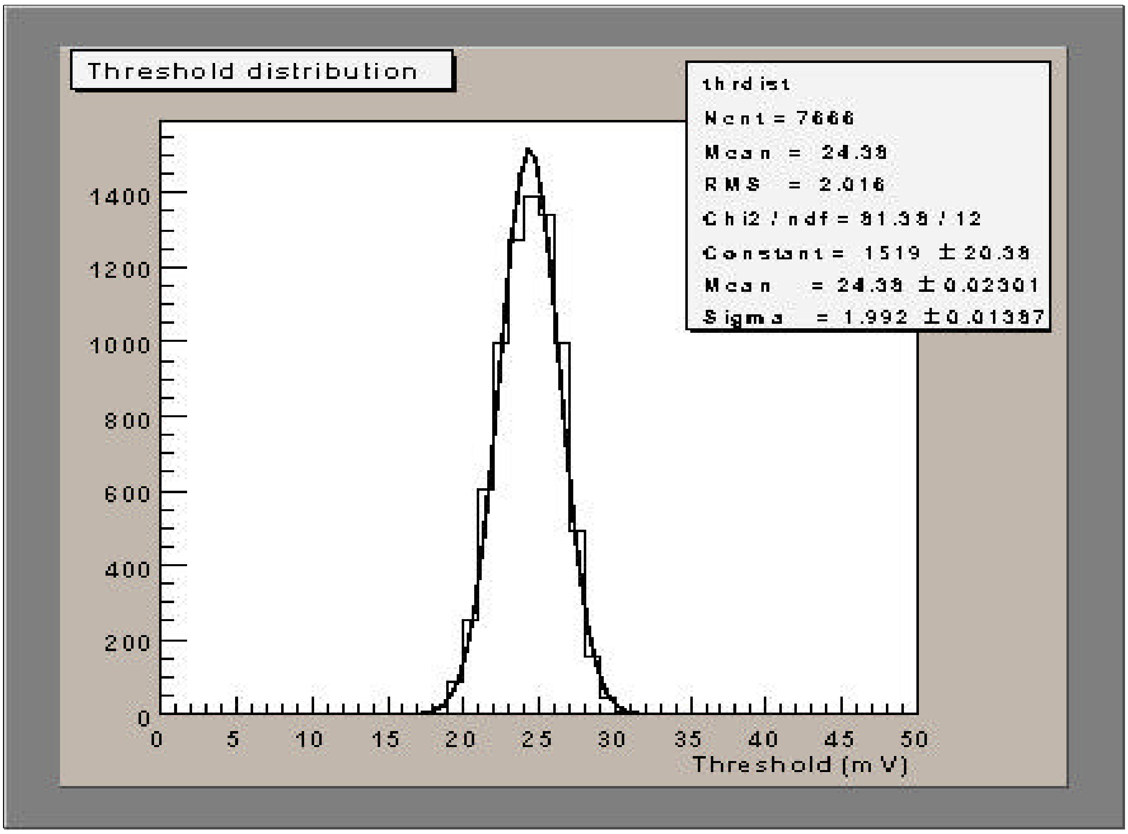
small problem with shape test pulse

-> non-homogeneous distribution

ALICE PIXEL DETECTOR

PRELIMINARY, CHIP ONLY

8000 pixels, threshold distribution



rms deviation ~2 mV = ? 150 e$^-$

absolute values need sensor

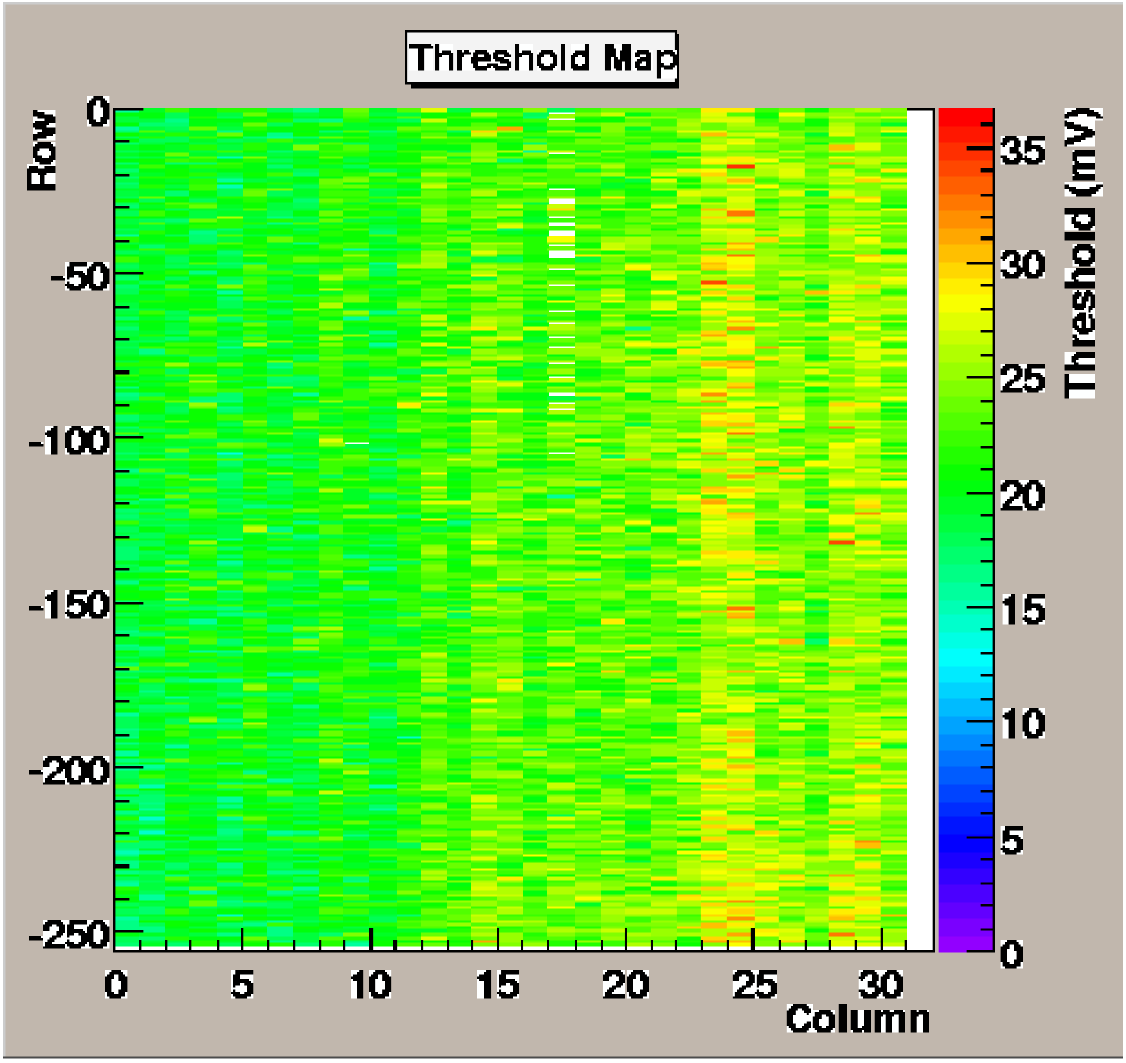
noise performance ~ 100 - 150 e$^-$ rms

power analog ~ 0.7 W

digital ~0.4 W whole chip

ALICE PIXEL DETECTOR

PRELIMINARY, with Si SENSOR



In - bump-bonded assembly

threshold ~22 mV = 1100 e^-

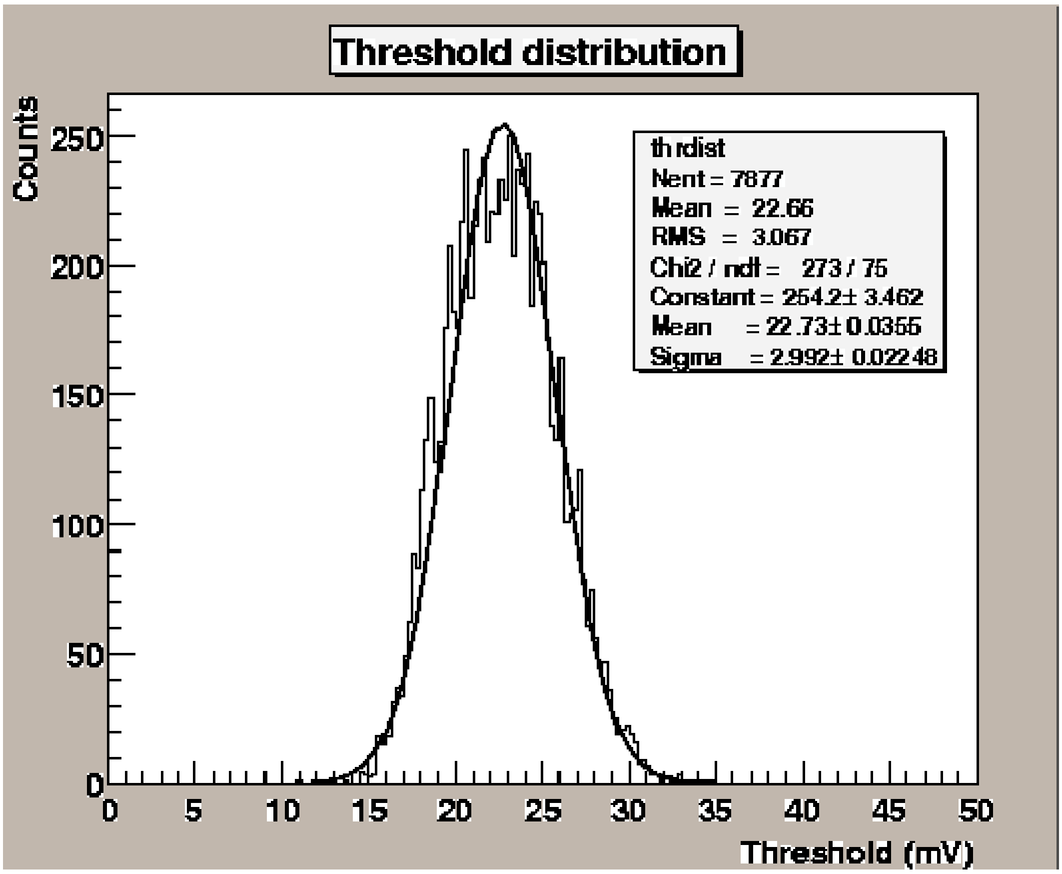
similar as without Si sensor

no threshold adjust applied yet

ALICE PIXEL DETECTOR

PRELIMINARY, with SENSOR

Threshold distribution



rms deviation ~2 mV = ? 150 e^-

No absolute calibration yet

noise performance ~ idem

IMPROVEMENT POSSIBLE

ALICE1 RESULTS (prelim)

THRESHOLD

MINIMUM VALUE ~800 e^-
with SENSOR ~1000 e^-

NOISE

~ 150 e^- rms

THRESHOLD SPREAD

150 e^- rms
COMPATIBLE with NOISE

TIMEWALK

<25 ns

200 e^- above threshold

DC LEAKAGE CURRENT

TOLERATES 200 nA / pixel
--> 0.5 - 1 mA cm^{-2}

RADHARD LAYOUT

WORKS UP TO 100 Mrad

THIN SENSORS

NOISE LEVEL & THRESHOLD in PIXELS COMPATIBLE with SMALL SIGNALS ~3000 e-h

OTHER COMPONENTS ALSO LOW MASS mechanics, cooling

THIN SENSOR IMPROVES PRECISION less scattering

better aspect ratio

fewer photon conversions

THIN Si SENSORS RADHARD

LOWER DEPLETION VOLTAGE

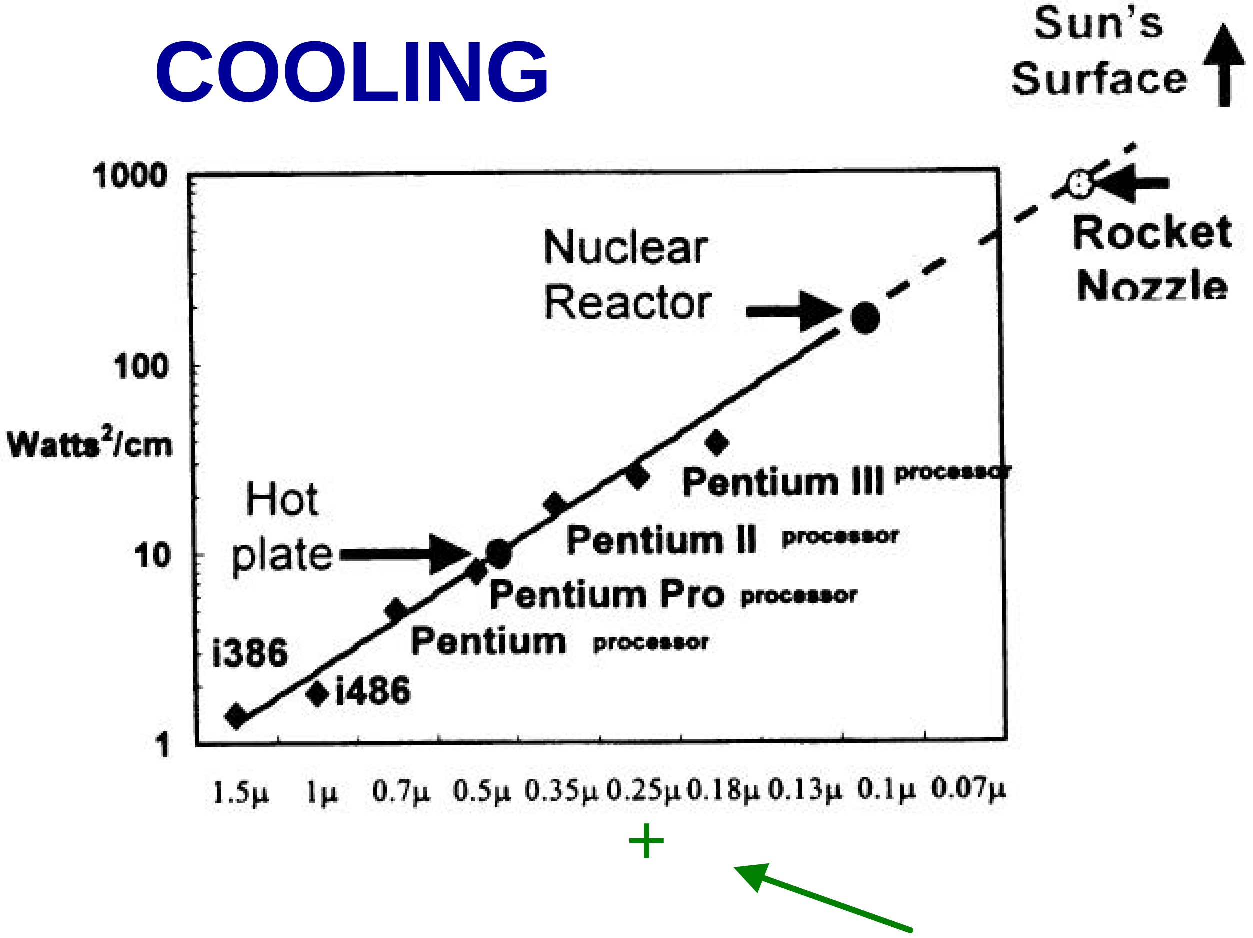
SHORT DISTANCE CHARGE COLLECTION

SMALL VOLUME - LOWER DARK CURRENT

LOW RESISTIVITY - LATE INVERSION

POWER DISSIPATION

PROCESSORS NEED COOLING



ALICE1 PIXEL CHIP 2.7 cm^2

USES 0.6 to 0.9 W + 0.3 W cm^{-2}

PIXELS vs Si MICROSTRIP

~3 kW m^{-2} **vs 0.2 - 0.6 kW** m^{-2}

CRYOGENIC OPERATION ?

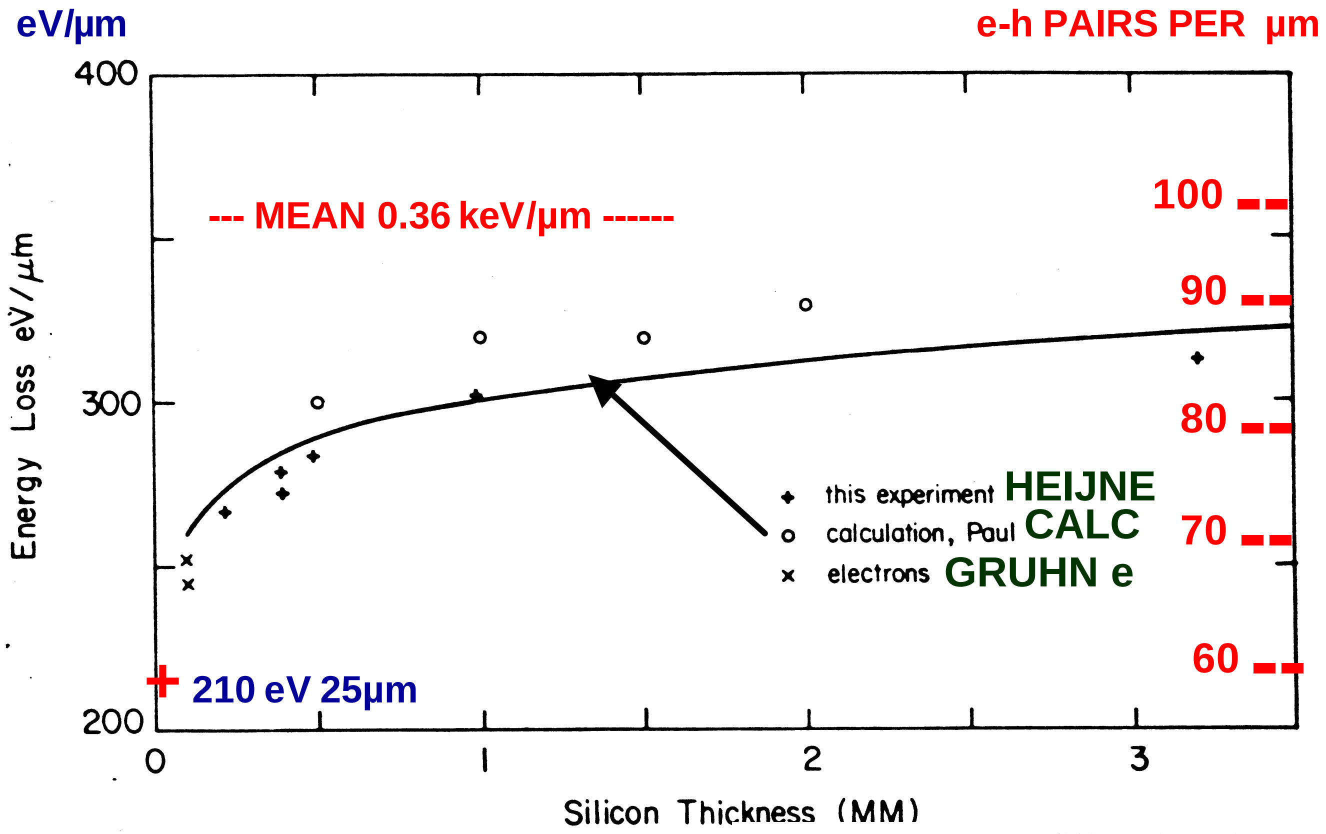
ENERGY LOSS
and
CHARGE CARRIERS
in THIN DEVICES

Erik HEIJNE

CERN EP- Div

ENERGY DEPOSITION in Si

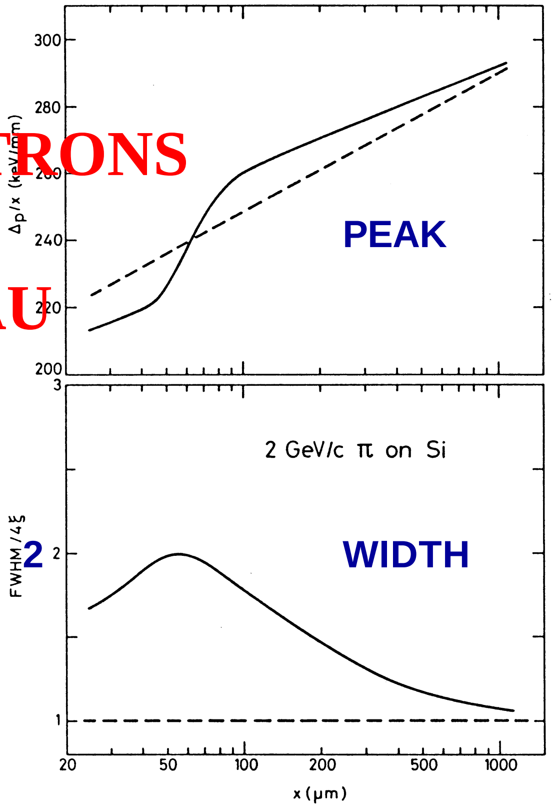
LOSS / µm DECREASES



Heijne CERN 83-06 (1983) 30

< 1mm BINDING of ELECTRONS causes

DEVIATIONS from LANDAU



Bak et al.
Nucl. Phys. B288 (1987) 681

THIN Si SENSOR : 50 µm

TENTATIVE CHARACTERISTICS

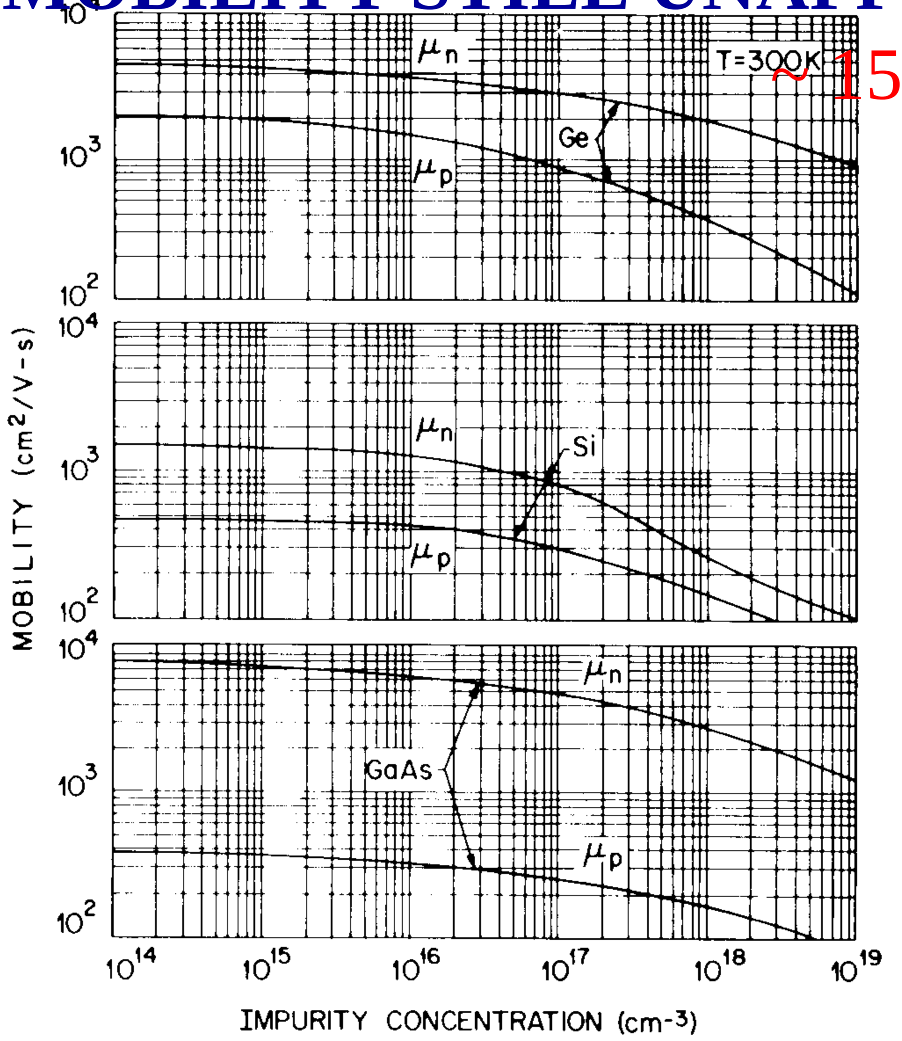
50 ? cm RESISTIVITY n-type 100 ? cm

Vdepl is 160 V 80 V

PIXEL 50 x 50 x 100 µm 10 fF to back

DOPING ~ 10^{14} cm^{-3} usually ~ 10^{14}

MOBILITY STILL UNAFFECTED

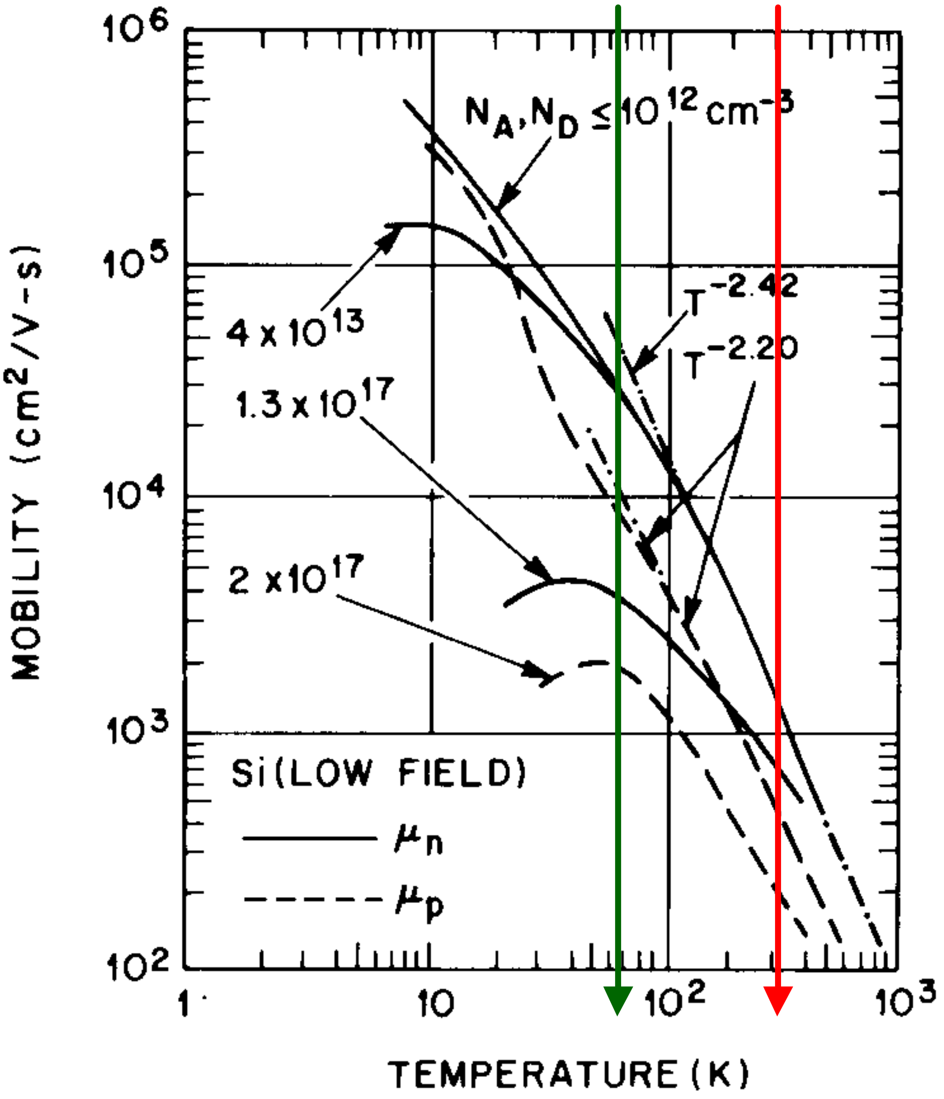


~1500 cm^2 V^{-1} s^{-1}

MOBILITIES in Si

MOBILITIES INCREASE ORDER of MAGNITUDE at 70K

MAYBE NOT NEEDED, BUT MANY CHARACTERISTICS IMPROVE with CRYOGENIC OPERATION



THIN Si SENSOR : 50 µm

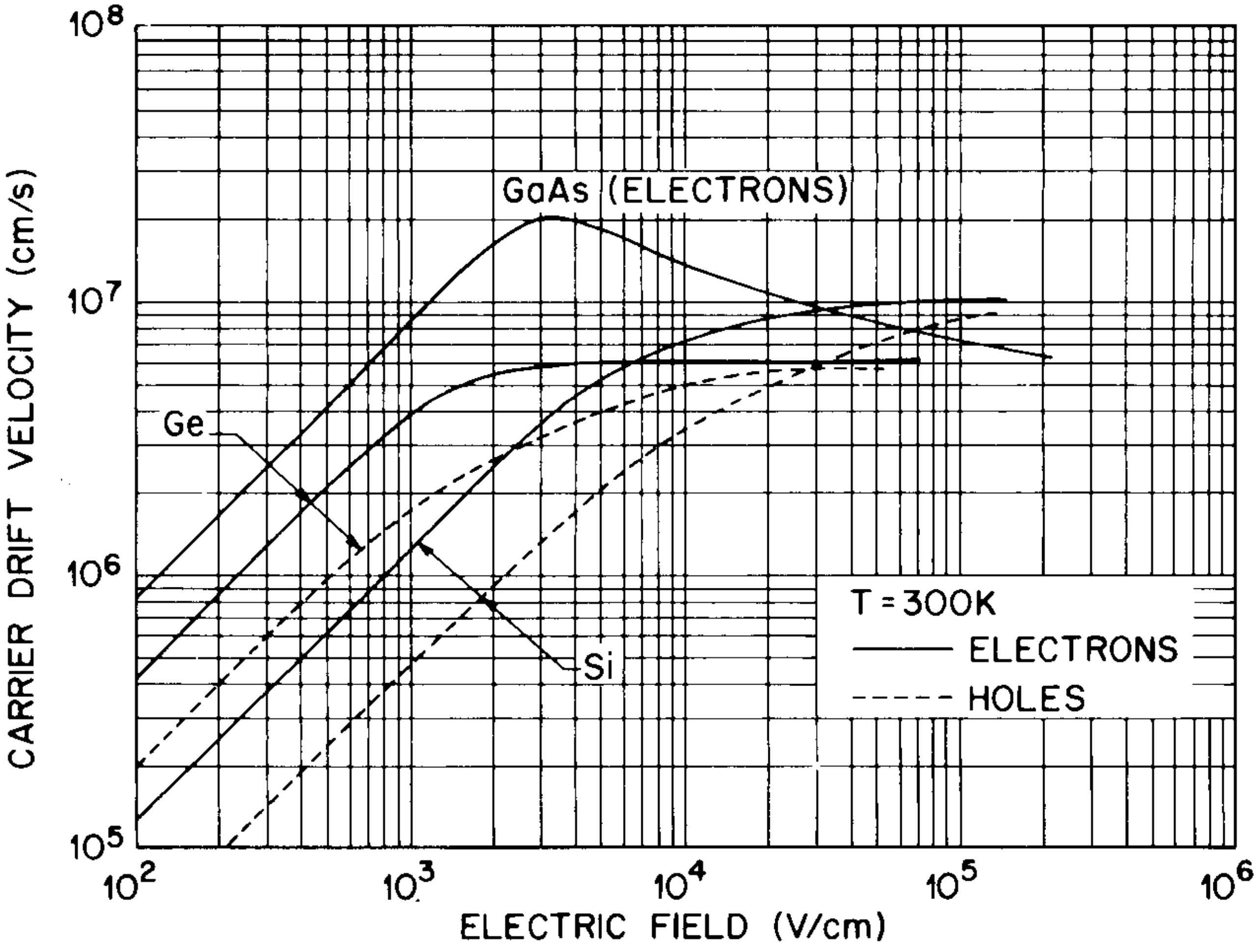
CHARGE SIGNAL 3000 $e^- h^+$pairs

ELECTRICAL FIELD 30 kVcm^{-1}

SATURATION VELOCITY at 10 kVcm^{-1}

electrons ~ 10^7 cm s^{-1}

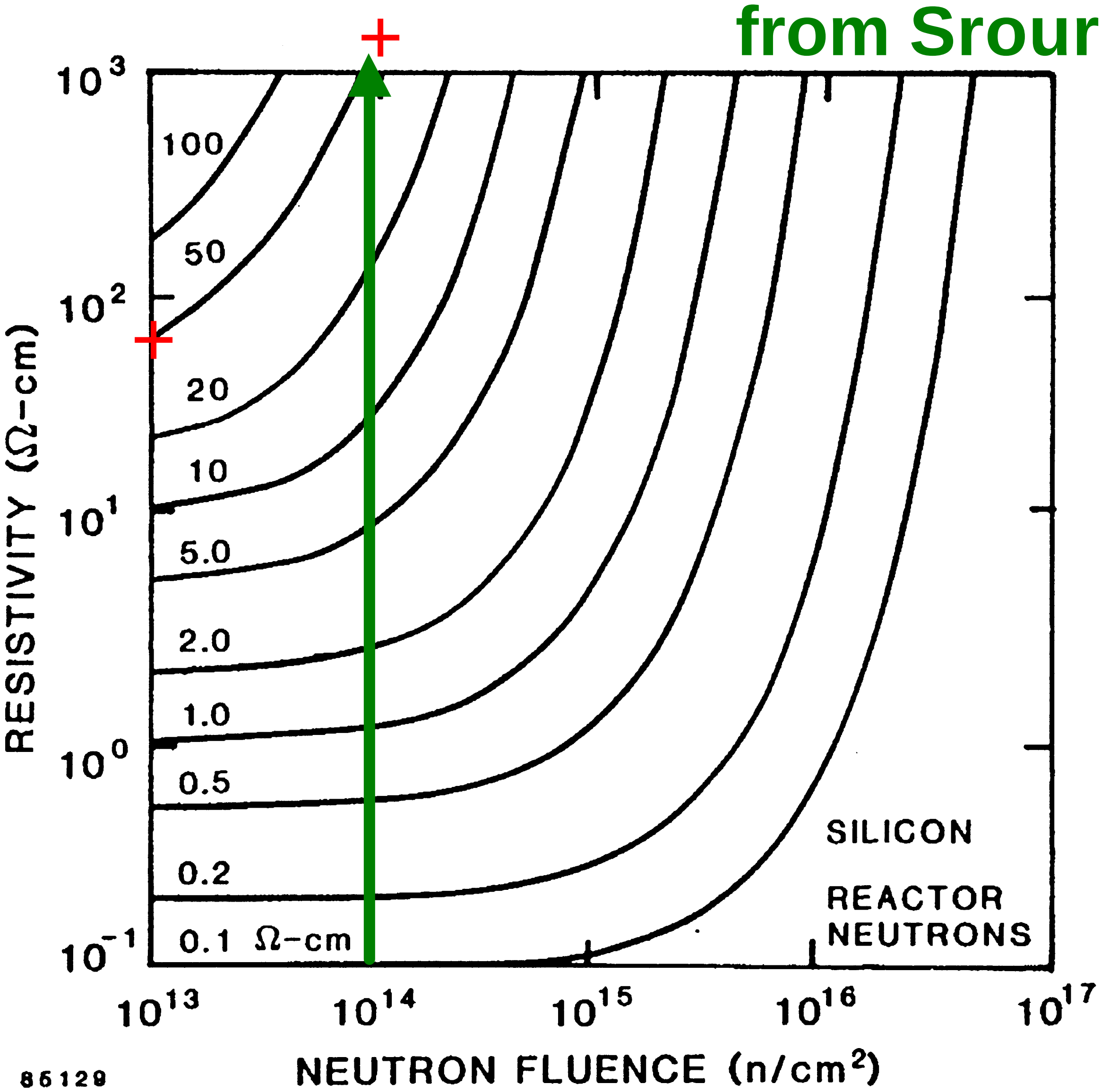
TRANSIT TIME e^-~0.5 ns h^+ ~2 ns



IMPROVEMENT of RADIATION HARDNESS

NEUTRON / HADRON IRRADIATION

CARRIER REMOVAL



from Srour

after 10^{14} n/cm^{-2}

\+ 50 ? cm --> 1000 ? cm

then $V_{depl} < 8V$

RADIATION HARDNESS

STARTING SILICON

50 ? cm - 100 ? cm

SLOWER TYPE INVERSION

EPITAXIAL LAYER on <1 ? cm ?

HAS TO BE STUDIED

BETTER CHARGE COLLECTION

SHORT TRANSIT TIME < 2 ns

LESS TRAPPING

DARK CURRENT ~ VOLUME

CAN BE COMPENSATED

UP TO mA cm^{-2}

READOUT can be RADHARD

DEEP SUBMICRON > 100 Mrad

TECHNOLOGY
for
THIN DEVICES

THINNING

THIN CHIPS are BECOMING COMMERCIALLY IMPORTANT

- SMART CARDS
- MEMORY STACKS (flash)

THINNING at WAFER LEVEL or AFTER ASSEMBLY

(eg LASER ABLATION)

READOUT CHIPS and SENSORS TREATED DIFFERENTLY

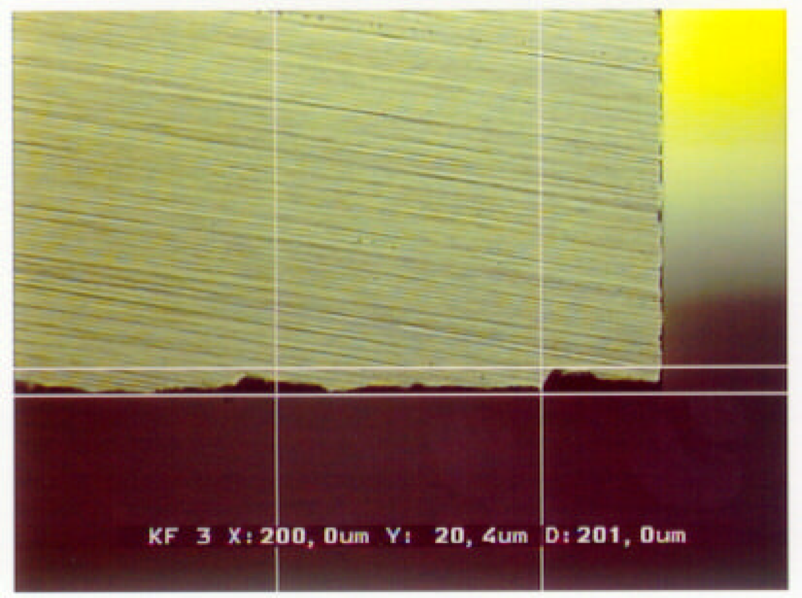
THINNING

BACK GRINDING of Si

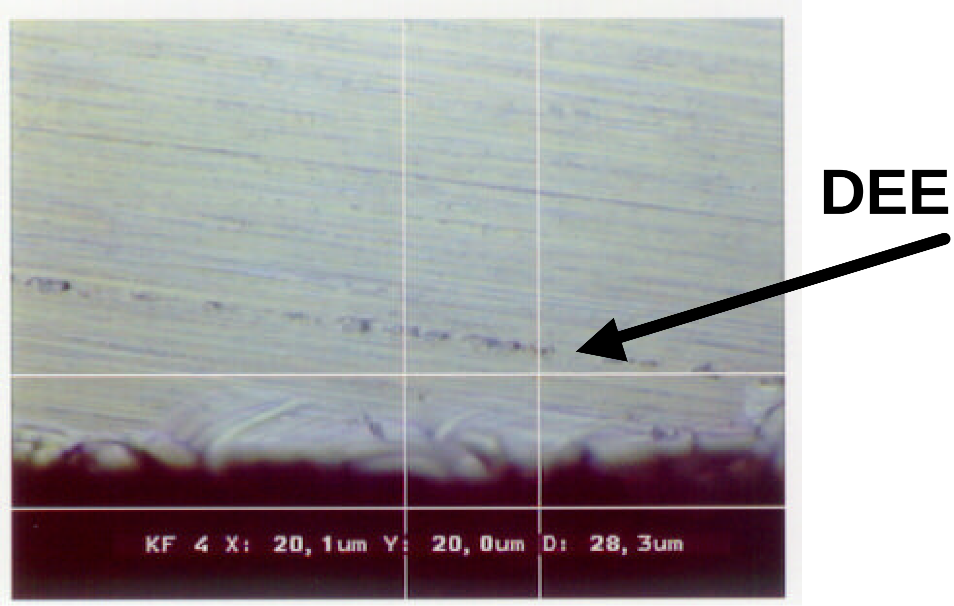
STANDARD OPERATION on WAFERS

USES QUARTZ or Si-Carbide POWDER

QUICK, down to ~ 150 µm



THINNED CHIP

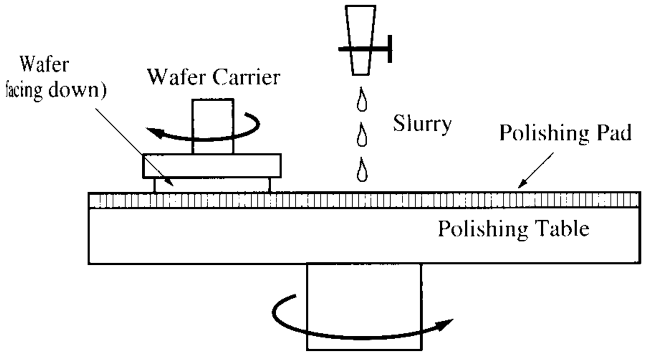


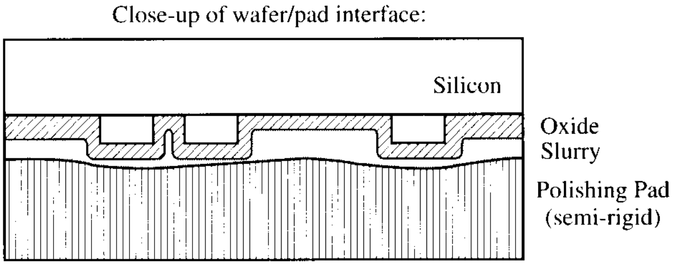
DEEP TRACKS

THINNING

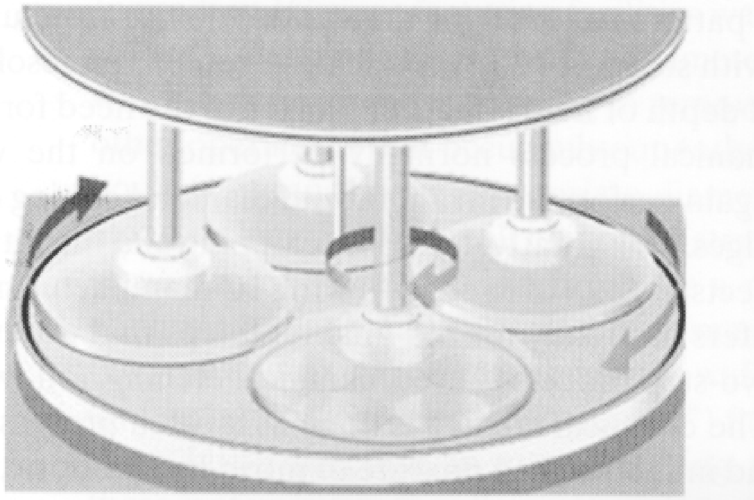
CMP -
CHEMICAL-MECHANICAL POLISHING

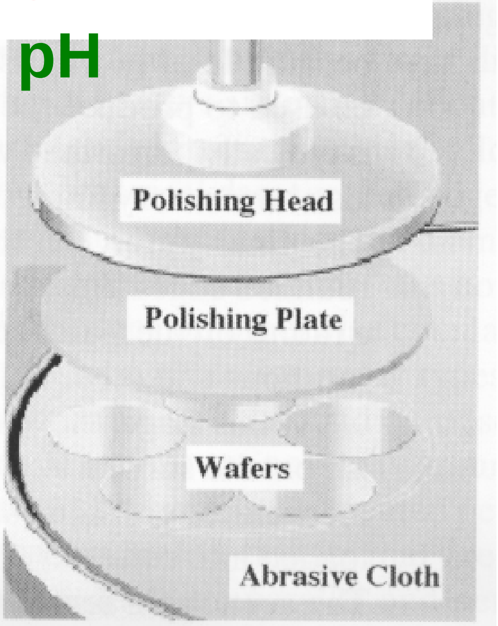
OXIDE or METAL SURFACE IS MADE





COLLOIDAL SILICA SLURRY with CONTROLLED pH

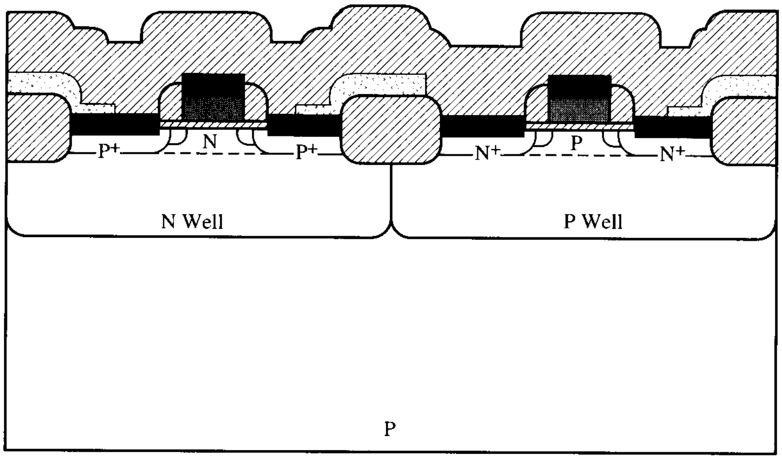




PLANARIZATION ESSENTIAL for DEEP SUB-MICRON

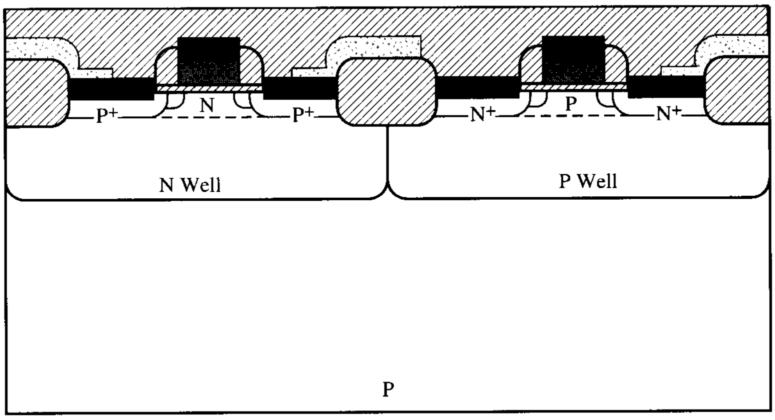
THINNING

CMP STEP in CMOS PROCESS

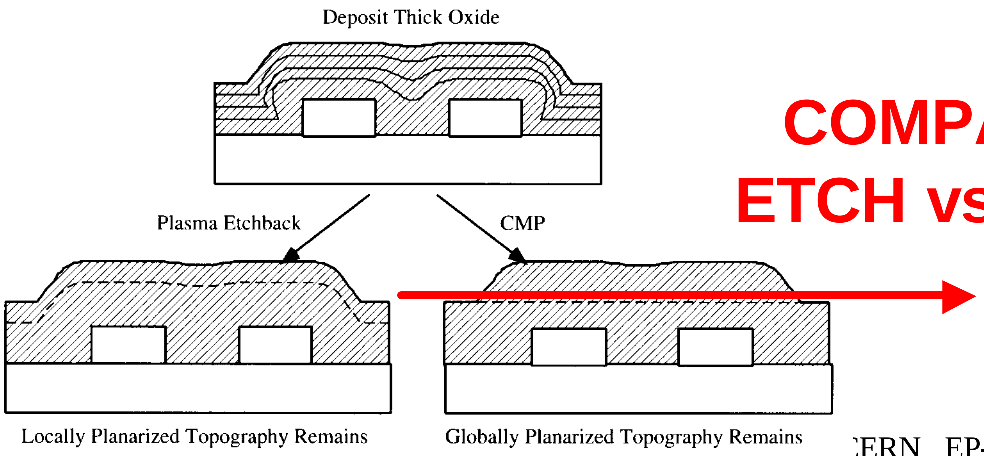


OXIDE

BEFORE CMP



AFTER CMP

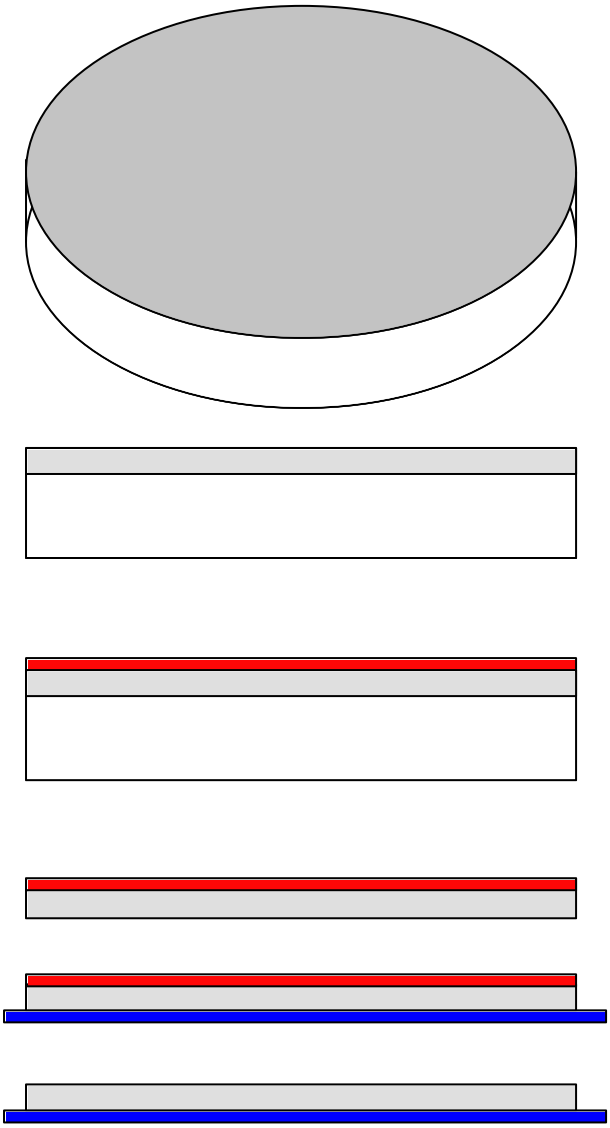


COMPARE ETCH vs CMP

THIN DEVICES

HANDLING IS PROBLEM

Solution: DBG : Dice Before Grind



PROCESSED WAFER
200 mm

PARTIAL SAW CUT

~40-60 µm

TOTAL ~725 µm

GLUE SPECIAL TOP FOIL

GRIND BACKSIDE WAFER

GLUE SUPPORT FOIL

TAKE TOP FOIL AWAY
USING UV
THIN CHIPS CAN BE USED

30 µm possible

TOSHIBA + DISCO + LINTEC

THIN SENSOR WAFERS

EPITA XIAL GROWTH on Si

HIGH RESISTIVITY SI on LOW r

silane VAPOUR DISSOCIATION

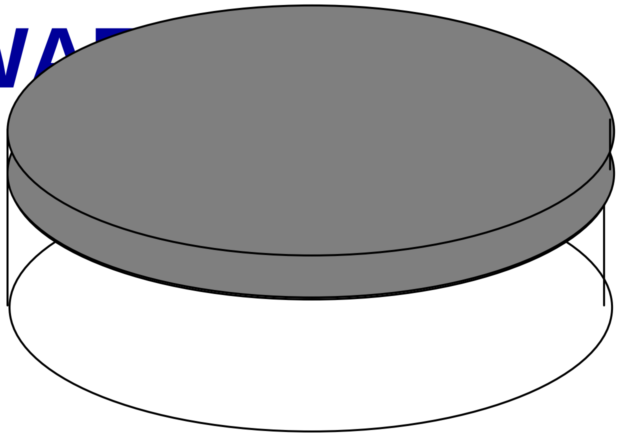
0.2 - 1.5 µm / min

950 - 1150 ºC

HIGH OXYGEN CONTENT

NO REAR CONTACT IMPLANT

POSSIBLE ON LARGE WA



2. GROW EPI LAYER

50 µm

1. LOW r Si

3. GRIND BACK

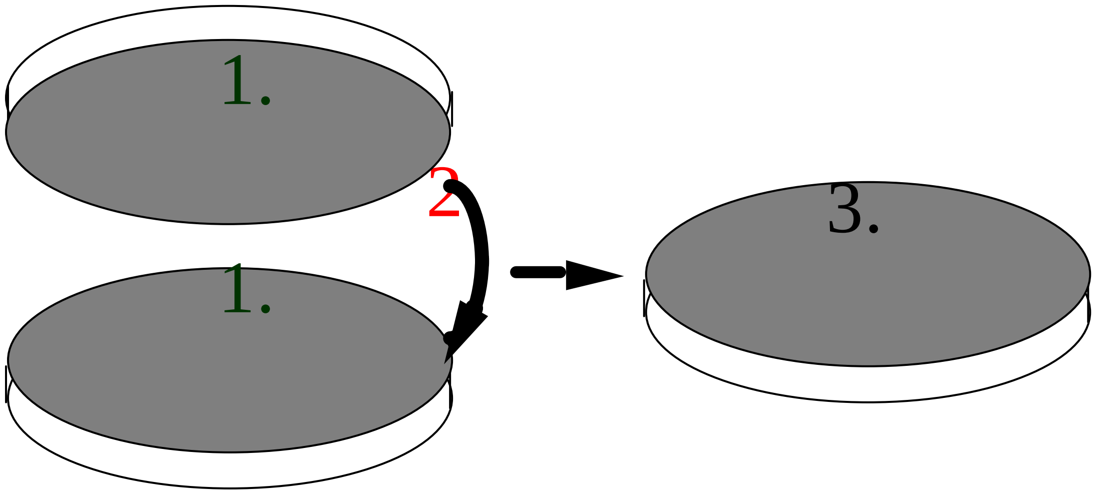
3 - D TECHNOLOGIES

SOI CMOS ‘Si on INSULATOR’

ACTIVE SI on ISOLATING

BURIED OXIDE

VARIOUS WAYS to MAKE SOI



1. OXIDIZE WAFERS
2. FUSE WAFERS <1000 ° C
3. GRIND-LAP-ETCH AWAY MOST of BACK
4. 2-4 μm for ACTIVE CMOS

STACK can be made by REPEATED OXIDATION-BACKLAPPING

3 - D TECHNOLOGIES

DEVELOPMENT of 3 - D is INSPIRED by NEED for MORE DENSITY

CAN IT BE USED for PHYSICS ?

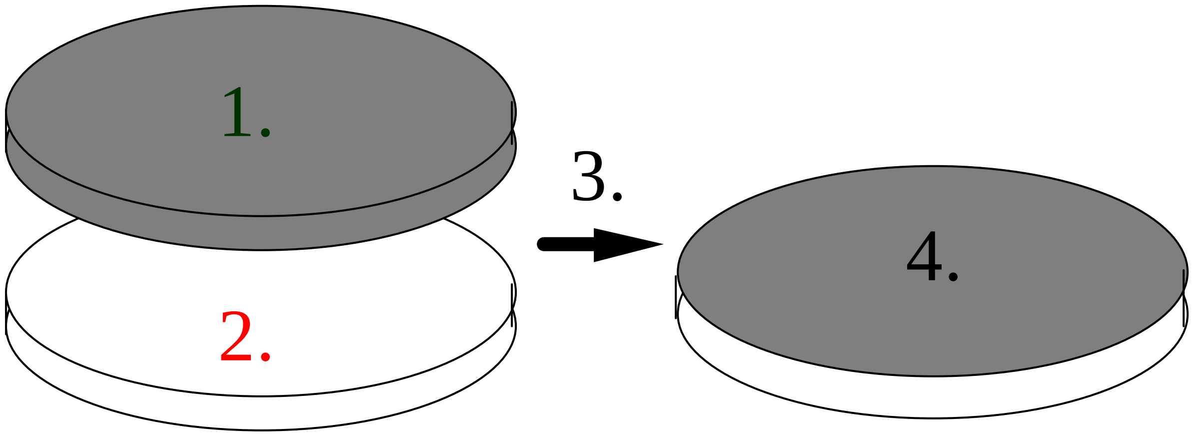
MORE ELECTRONIC FUNCTIONS per UNIT of AREA

MULTIPLE DETECTION LAYERS ‘TRACK VECTOR DETECTORS’

OTHER ??

3 - D TECHNOLOGIES

Si on Anything : SOA



1. **SOI wafer** with **BURIED OXIDE**
   carries bipolar and/or CMOS
   FACE DOWN
2. **'ANYTHING'** eg **GLASS**
   insulating substrate
3. **GLUE TOGETHER**
4. **REMOVE Si SUBSTRATE**

low parasitics, perfect isolation, low power

2.5 GHz for low power RF receiver

(Philips, Proc. IEEE 88(2000) 1546)

TECHNOLOGY THIN DETECTORS

LOW MASS SENSORS

- 100 µm to 150 µm Si
- DIAMOND
- EPITAXIALSi : 80 µm on low ž

THINNED READOUT CHIPS

- SMART CARDS TECHNOLOGY
- LOW NOISE by SEGMENTATION

MULTI-CHIP-MODULE

- SENSOR is the SUPPORT
- BUS and POWER INTEGRATED
  - Cu 2-8 µm, BCB 3-10 µm
  - 3 - 5 LAYERS
  - LINEWIDTH 10 µm, PITCH 20 µm
  - VIA nominal 10 µm , PITCH 50 µm
  - BUMPS besides staggered VIAs

CONCLUSION

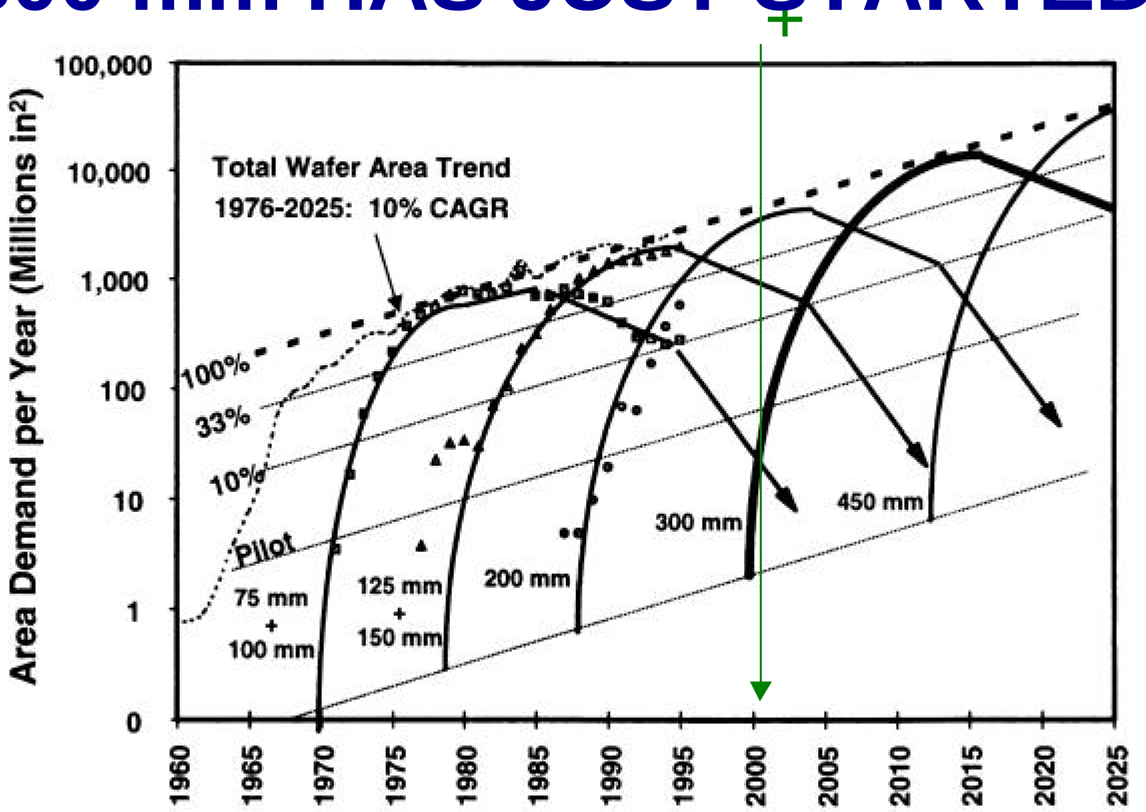
CHIP TECHNOLOGIES +
ASSEMBLY TECHNOLOGIES
FOLLOW DEVELOPMENTS in INDUSTRY
--> NEW DETECTORS
NEW
APPROACHES

USING LOW-NOISE,
FAST PIXEL READOUT CHIPS :
DIFFERENT OPTIMI ZATION ??

FAST, PRECISE,
RADHARD TRACKER
LARGE IMPROVEMENTS POSSIBLE
MANY PROBLEMS
HAVE TO BE SOLVED

Si WAFER SIZE

300 mm HAS JUST STARTED



FACTORY INVESTMENT >> B$

NEW CMOS LINKED TO LARGE WAFERS / LARGE VOLUME

SPECIAL HARDWARE & LOGISTICS for SMALL VOLUME ORDERS

CAN BACK-END PROCESSING FOLLOW ?

SYSTEM MANAGEMENT

VARIETY of FUNCTIONS MAY BE IMPLEMENTED on SENSOR READOUT CHIPS

POWER DISTRIBUTION

LASER DRIVEN POSITIONING

TEMPERATURE SENSOR

MAGNETIC FIELD SENSOR ?

OTHERS ???

CMOS COMPATIBILITY NOT GRANTED

PACKAGING TECHNOLOGIES can be used in PARTICLE PHYSICS

HYBRIDIZATION using SENSOR as SUBSTRATE

SPECIAL CONSTRAINTS

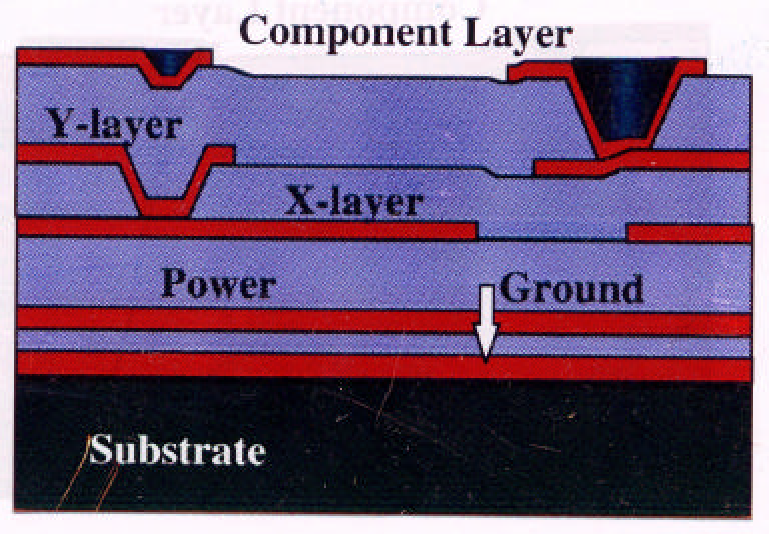
THIN, 'LOW MASS' ASSEMBLY POSSIBLE

MCM - D

Multi Chip Module DEPOSITED

on CERAMIC

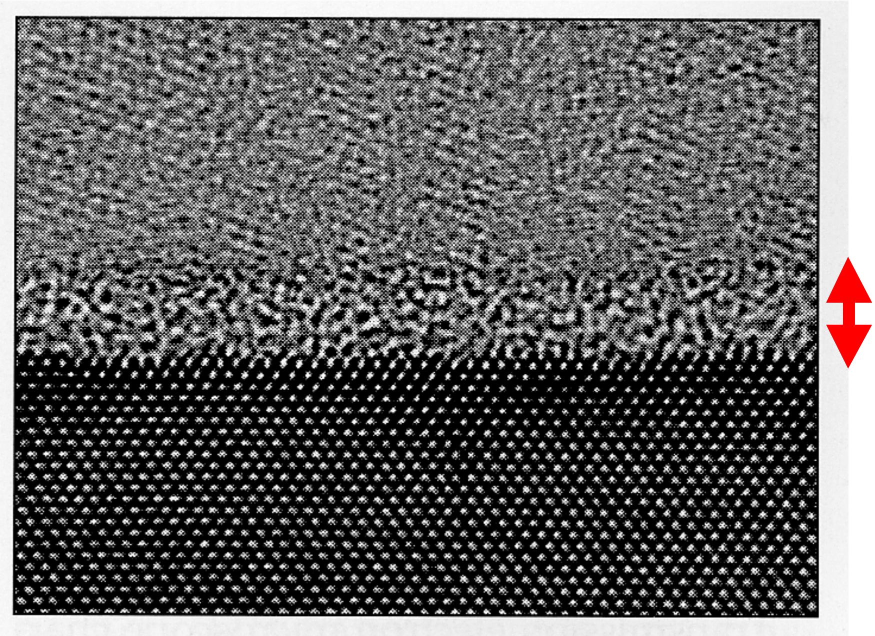
on Si



IMEC
Leuven

Impact Deep-submicron CMOS for ADVANCED detector readout

MOS Gate TEM Bell Labs April 2000



Poly Si

SiO_2 **1.6 nm**

Si

Reliable oxides can be made already with only ~ 6 atoms in SiO_2 layer

SiO_2 CMOS technology used
for 0.08 µm --> 0.02 µm? transistors
--> "Noon Lecture" by TAUR

Thin gate oxide (< 8 nm) also is unaffected by radiation (test > 30 Mrad)