



# **Micromachining of microchannels in silicon**

**for cryogenic cooling purposes**

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**20th January 2003**



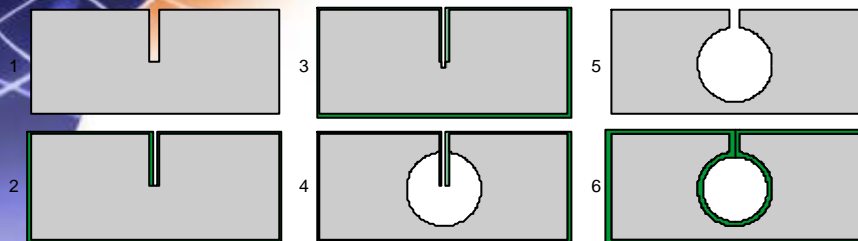
## **Outline**

- Buried microchannels in silicon
  - micromachining process
  - silicon nitride type
  - application: micropipette
  - polysilicon type
- Cryogenic detector cooling using buried microchannels
  - thermal stability
  - fluidic connections
  - flow control (pumping, sieving)
- Patent situation
  - buried channels
  - semiconductor cooling with integrated microchannels



## Microchannels buried in a silicon wafer

### Buried channel process

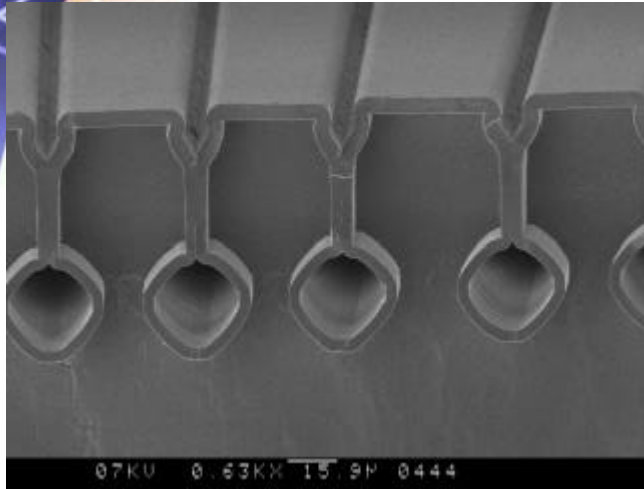


See: animation of buried channel process  
(courtesy of Oxford Instruments)

[http://www.oxfordplasma.de/process/si\\_sinch.htm](http://www.oxfordplasma.de/process/si_sinch.htm)



# Silicon nitride type



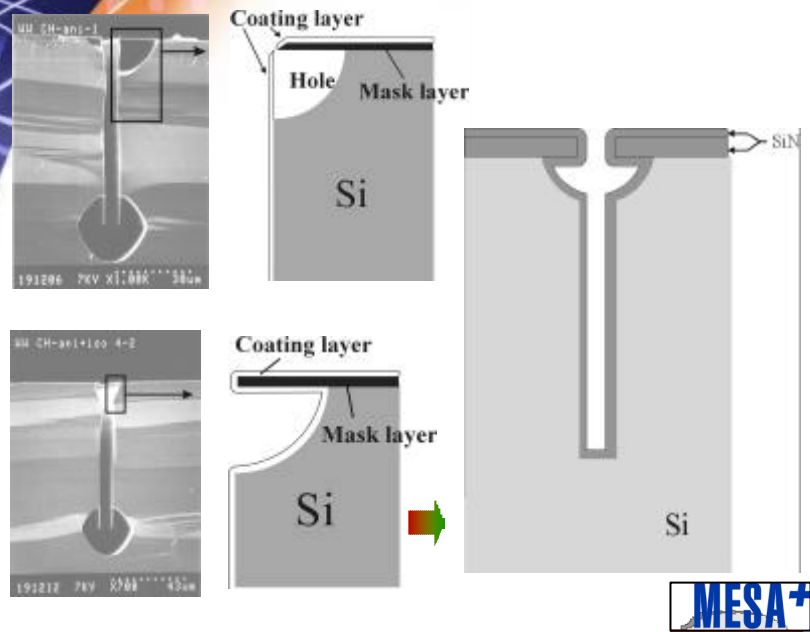
## Different profiles of buried channels

M.J. de Boer et al.  
 J. MEMS 9, 2000, pp. 94-102

Table 1. Different process solutions for BCT

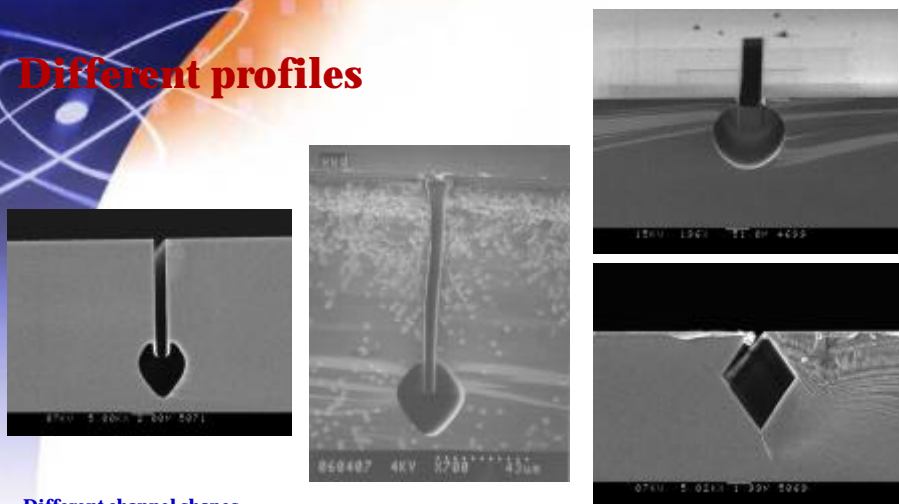
Step	Wafer 1	Wafer 2	Wafer 3	Wafer 4
1. Buried channel	Etching: 500 RIE	Etching: 500 RIE	Etching: 500 RIE	Etching: 500 RIE
2. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
3. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
4. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
5. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
6. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
7. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
8. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
9. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
10. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
11. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
12. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
13. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
14. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
15. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
16. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
17. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
18. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
19. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>
20. Buried channel	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>	Deposition: SiO <sub>2</sub>

## Process problems & solutions



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## Different profiles

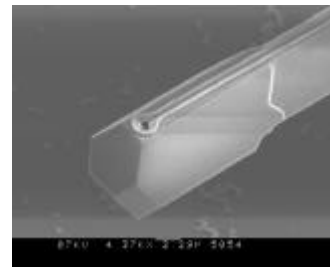
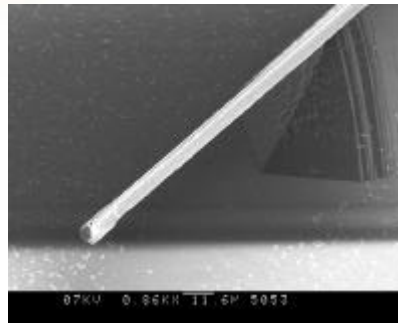
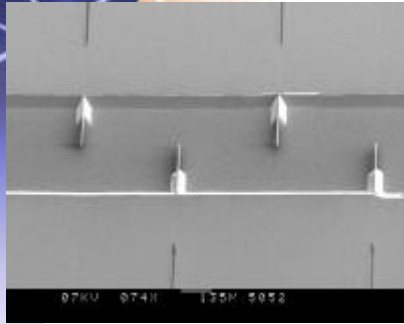


### Different channel shapes

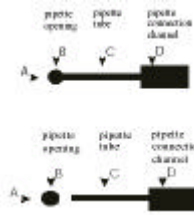
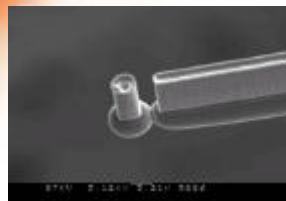
- (a) Left: obtained by isotropic RIE
- (b) Center: obtained by electrochemical etching in 5% aqueous HF solution
- (c) Right, top: obtained by etching in HF-HNO<sub>3</sub> solution
- (d) Right, bottom: obtained by etching in KOH solution.

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# Micropipettes for DNA studies



C. Rusu et al.,  
J. MEMS 10, 2001, pp. 238-246



mask type I

mask type II

mask type I

mask type II

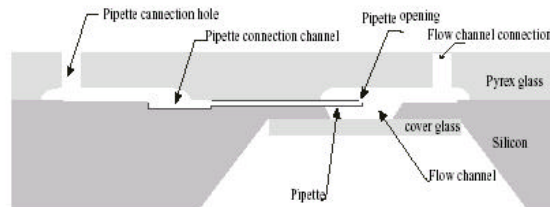
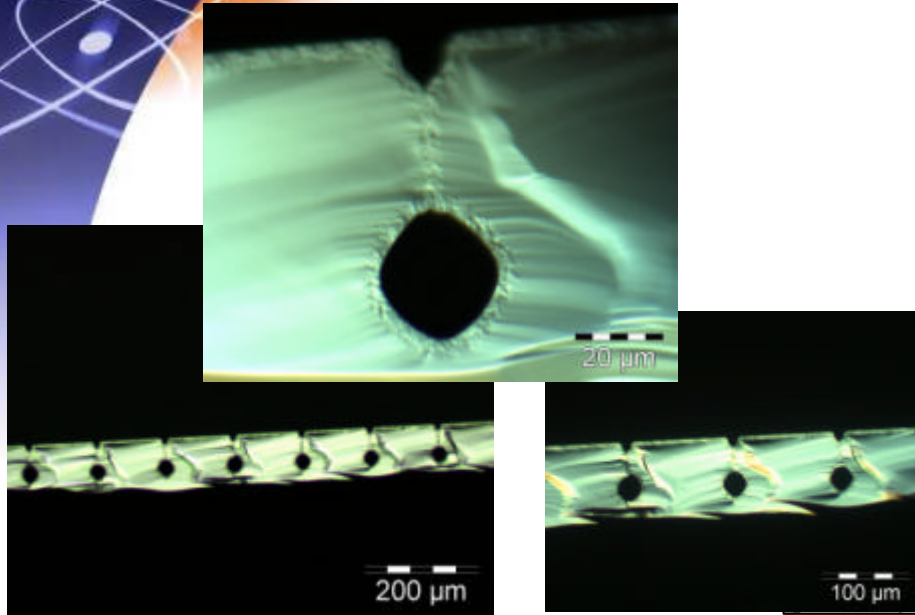


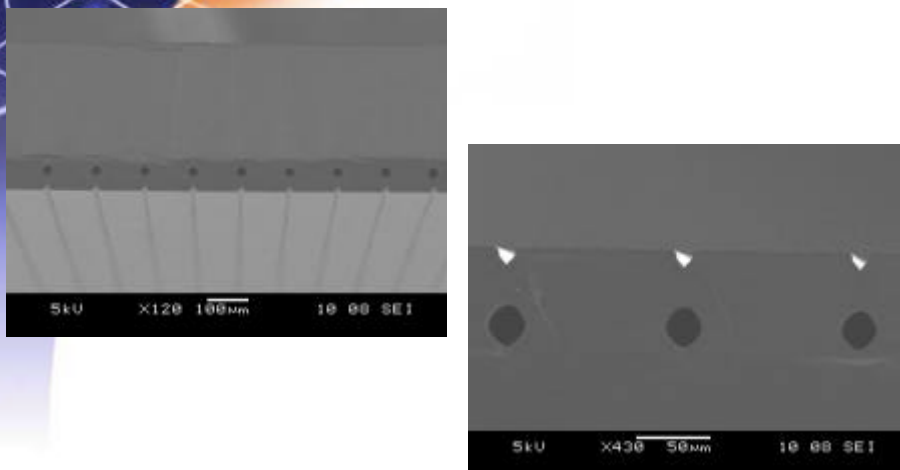
Fig. 3. Cross section of a flow cell consisting of integrated micropipette in a flow channel.



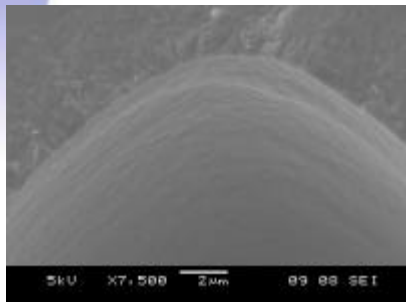
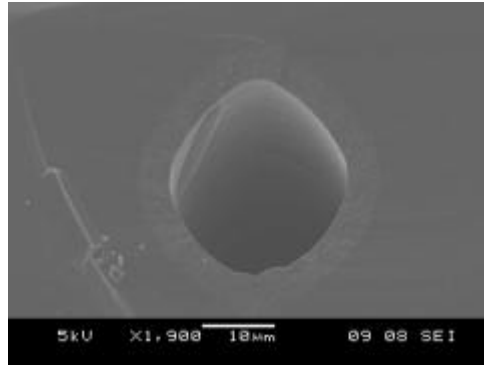
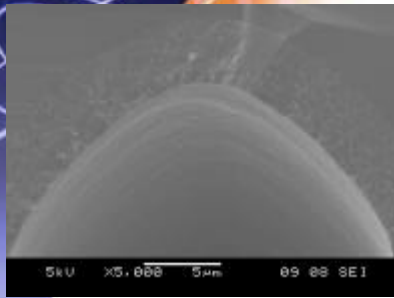
## Polysilicon microchannels (opt. microsc.)



## Polysilicon microchannels (SEM)



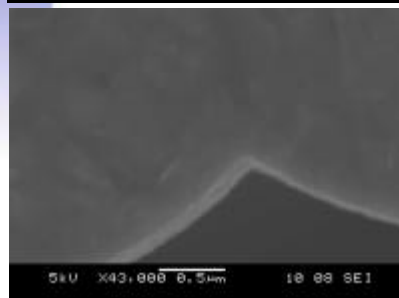
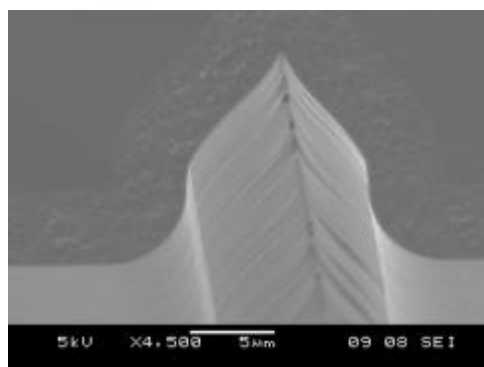
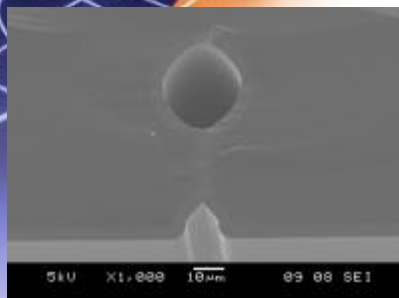
## Polysilicon microchannels (SEM)



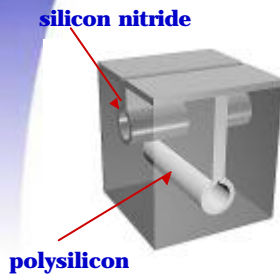
**Inner diameter channel: 27- 30 microns**  
**Center of channel positioned 54 microns below the wafer surface**  
**Poly-Si layer thickness: 3.4-3.6 microns inside channel, 4.9-5.1 microns on top surface**



## Polysilicon microchannels (SEM)



## Polysilicon vs. silicon nitride



Parameter	'low-stress' $Si_3N_4$	Poly-silicon
Gases (100 %)	$SiH_2Cl_2 : NH_3$	$SiH_4$
Gas flow ratio (sccm)	70 : 18	50
Deposition temperature (°C)	850	590
Pressure (mTorr)	200	250
Deposition rate (nm/min.)	8.3	4.48
Maximum layer thickness <sup>a</sup> (µm)	2.5	5
Stress (MPa)	300	very low
Etching rate ( in step 6) (µm/min)	0.01-0.05	1-5

<sup>a</sup> the maximum thickness is the layer thickness that can be deposited in an acceptable time, e.g. one day.



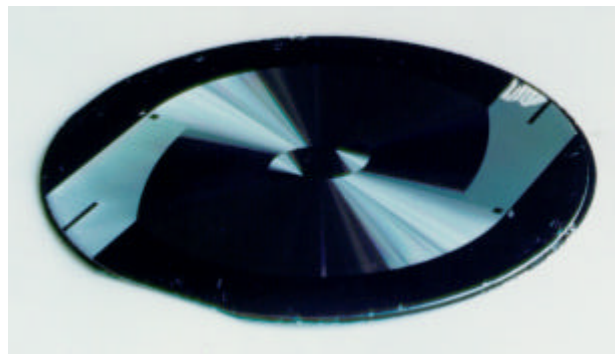
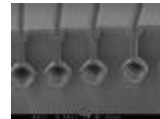
## Microchannel for gas chromatography



**bonded wafer pair**  
problem: misalignment



**surface micromachined**  
problem: non-circular, only low pressure



**buried microchannel: circular cross-section, smooth walls**  
problem:  $SiN$  stress leads to wafer curvature





# Cryogenic cooling of silicon detectors using buried microchannels?

## Thermal stability

- residual stresses: silicon nitride / polysilicon
- thermal expansion coefficients

- polysilicon: basically the same as Si X-tal:

Temperature (K)	100	200	400	1000
Lin.Coeff. Therm. Exp. ( $10^{-6}/K$ )	0.5	1.1	2.7	4.7

- LPCVD silicon nitride: 2.3 (stoichiom.) - 4 (Si-rich)  $10^{-6}/K$

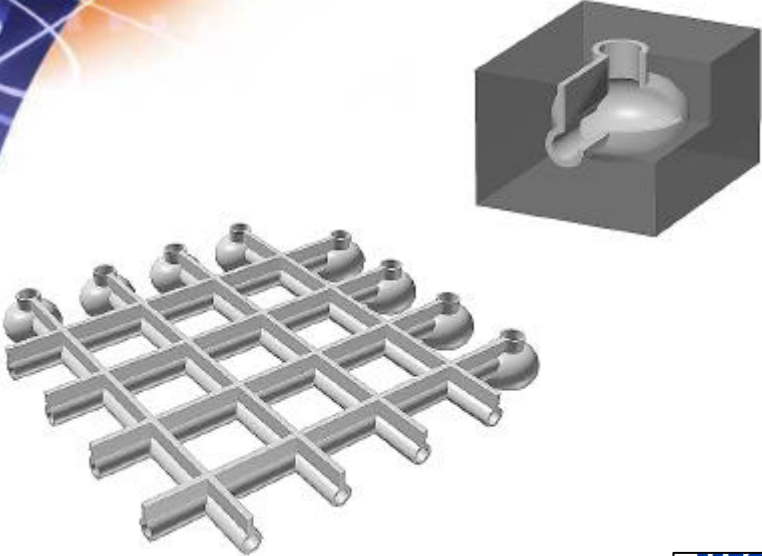
- annealing of polysilicon on Si: gives "epitaxial" regrowth



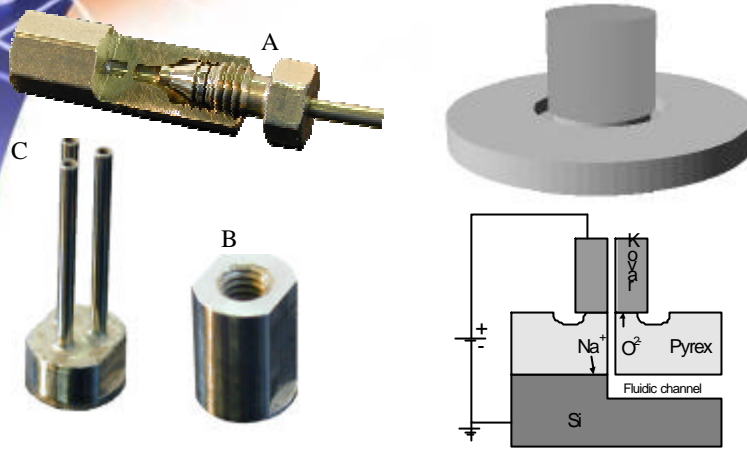
# Fluidic connections and integration of components

Some examples

## Buried channels with etched inlet



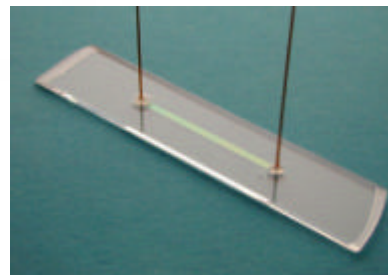
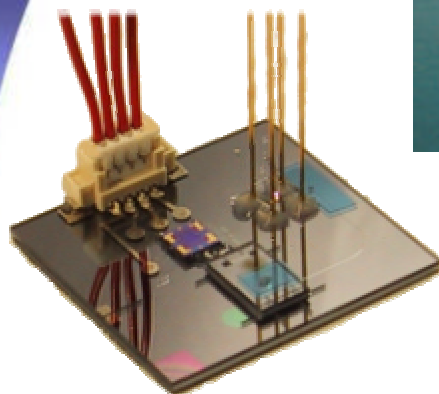
## Local (anodic) bonding of Kovar to Pyrex



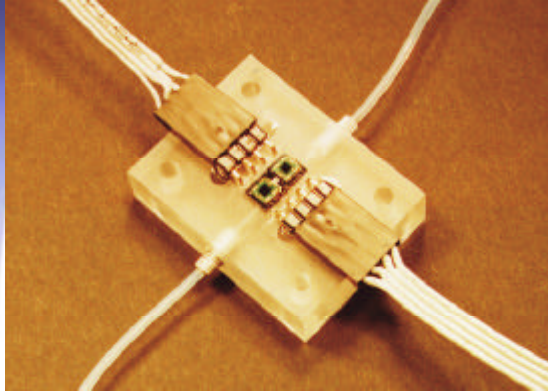
M.T. Blom et al., J. Micromech. Microeng. 11 (2001) 382



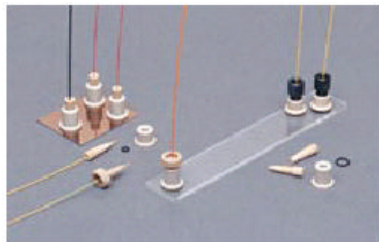
## Glued capillaries?



## Connections in PMMA block



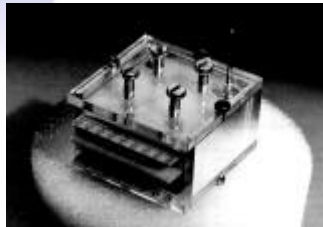
## UpChurch Nanoports



## Ways of integration

### Modular

- Flexible component design
- Small series
- Standard pick&place
- Mixed technology
- **Interconnections**



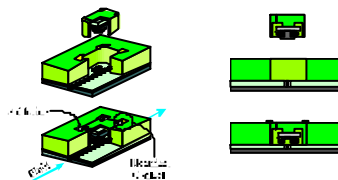
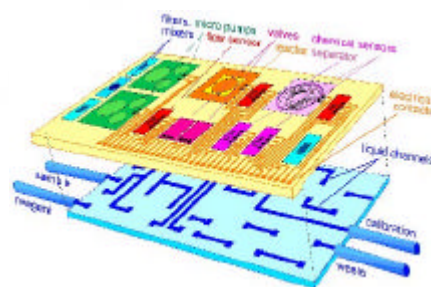
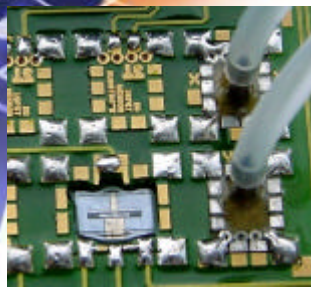
**Vertical stacking**  
 Institute of Microtechnology (IMT)  
 University of Neuchâtel, Switzerland

### Monolithic

- Small dead volumes
- Suited for large(r) series
- **Design constraints**
- **Decreasing yield with nb. components**

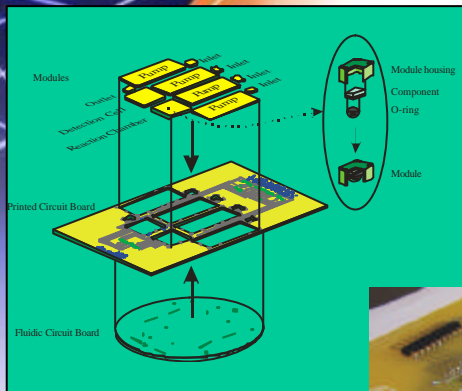


## Modular Assembly TAS



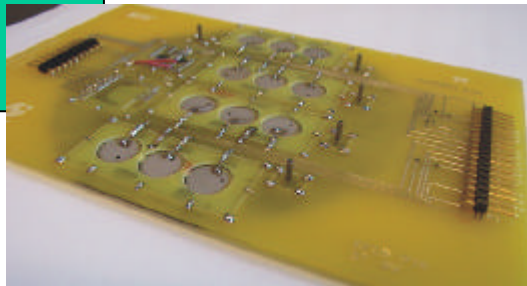
"MATAS" by Lionix B.V. (formerly 3T BV), Enschede, NL



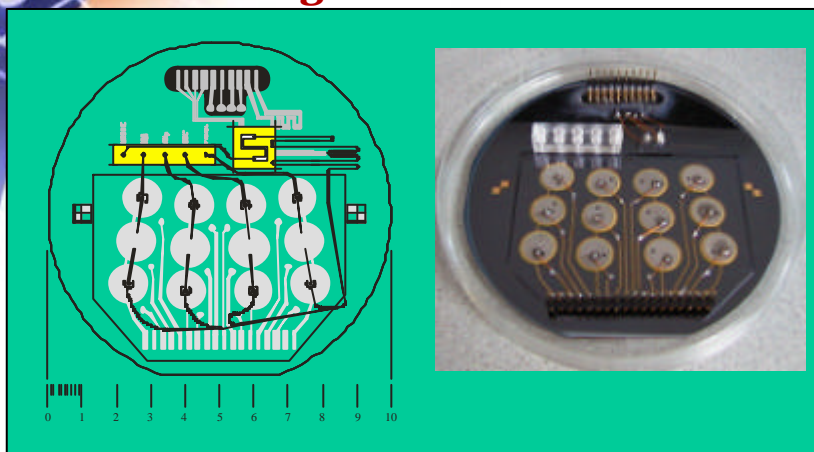


## Modular assembly

MATAS (Lionix BV / 3T BV)

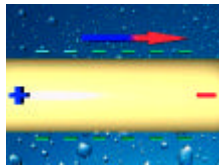


## Monolithic design

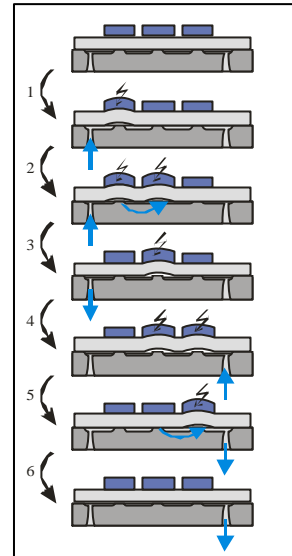
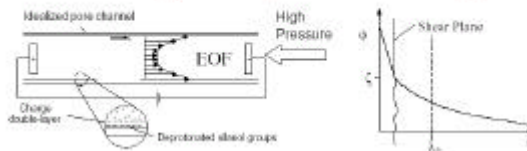


## Fluidic control

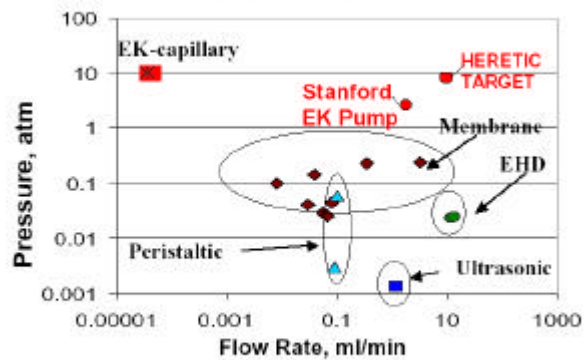
- micropumps
  - piezoelectrically driven?
  - EOF (elektrokinetic)?



### Working Principles of EK Pumps



## Micropump Technology Overview



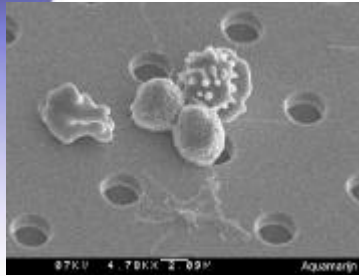
S. Shoji and M. Esashi, J. Micromech. Microeng 4, 157, 1994.

P. Gravesen, J. Branebjerg and O. S. Jensen, J. Micromech. Microeng 3, 168, 1993.

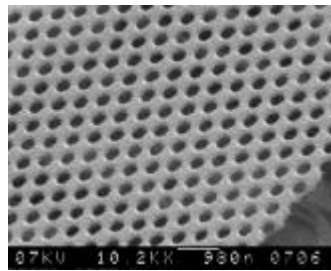
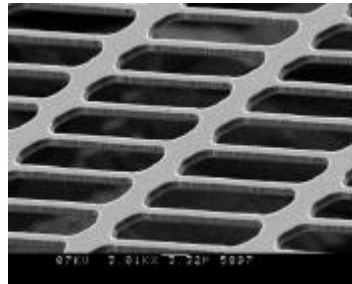
from: DARPA HERETIC Program



## Micromachined filters?



Source: Aquamarijn Micro Filtration, The Netherlands



## Patent situation

**US 4993143 D.W. Sidner et al., Mar. 27, 1990:**

**Method of making a semiconductive structure useful as a pressure sensor**

**(describes process of making buried channels; sealing by lateral epitaxial silicon growth, to my knowledge oldest patent on this topic)**

**US 5210440 J.M. Long, Jun. 3, 1991:**

**Semiconductor chip cooling apparatus**

**(chip die on support surrounded by flowing cooling fluid)**

**US 6254214 A. Murthy et al., Jun. 11, 1999:**

**System for cooling and maintaining an inkjet print head at a constant temperature**

**(channels etched from both sides of wafer)**





**Two recent patents of ST Microelectronics:**

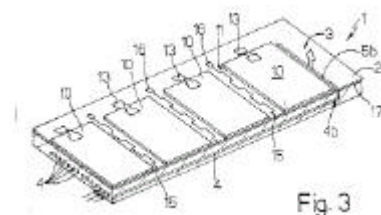
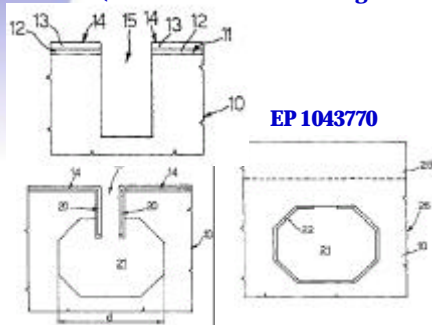
**EP 1043770 G. Barlocchi et al., Oct. 11, 2000 (priority Apr. 9, 1999):**

**Formation of buried cavities in a monocrystalline semiconductor wafer  
(sealing by lateral epitaxial silicon growth)**

**EP 1123739 U. Mastromatteo et al., Aug. 16, 2001 (priority Feb. 11, 2000):**

**Integrated device for microfluid thermoregulation , and manufacturing  
process thereof**

**(buried channels as cooling channels for PCR device)**



EP 1123739

