SOLDER BUMP FLIP CHIP
BONDING FOR PIXEL DETECTOR
HYBRIDIZATION

Jorma Salmi and Jaakko Salonen

VTT Information Technology
Microelectronics
P.O. Box 1208
FIN-02044 VTT, Finland
(visiting: Micronova, Tietotie 3, Espoo)

Wednesday, June 11th, 2003
Outline

• Logistics
• Bumping Process
• Facilities/Equipment
• Thinning of Wafers
• Flip Chip Assembly
• Application Example: CERN ALICE Assembly
• Yield Factors
• Shortlist of Things
• Future Trends
• Summary
Logistics

Design at CERN

200-mm (8")
Readout Wafers from IBM

Bumping layout rules

Testing (probing) at CERN

125-mm (5")
Detector Wafers from Canberra

Hybridization at VTT

Final Testing & Application at CERN

Feedback
Process Steps for Hybridization at VTT

- Solder Bumping of Readout Wafers
- Solderable Pads on Detector Wafers
- Optional Thinning of (Readout) Wafers
- Dicing
- Flip Chip Bonding
Flip Chip Process: Key Features

- 200-mm (8”) wafer capability.
- Tin-lead solder alloy bumps are used for mechanical strength of bonded assemblies.
- Bump deposition by electroplating.
- Process is compatible with wire bonding pads and unpassivated backside metallization.
- Thinning (back grinding) of bumped readout wafers.
- ‘Clean’ dicing with front side protection using either photoresist or tape.
- Fluxless flip chip bonding.
Bumping Process

1. Contact pad metal (typically Al)

2. Cu TiW Field metal deposition

3. Exposed & Developed Photoresist

4. Plated solder alloy (Eutectic Sn-Pb)
   Under Bump Metallurgy (typically plated Ni)
Bumping Process [cont’d]

5. After photoresist stripping
6. Wet etching of field metal Cu
7. Solder reflow
8. Wet etching of field metal TiW
## Processes/Equipment at VTT

<table>
<thead>
<tr>
<th>PROCESS</th>
<th>EQUIPMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photoresist coating</td>
<td>Suss MicroTec ACS200</td>
</tr>
<tr>
<td>Mask Aligners</td>
<td>Suss MicroTec MA6 &amp; MA200CC</td>
</tr>
<tr>
<td>Thin film sputtering</td>
<td>Von Ardenne CS730S, MRC 903</td>
</tr>
<tr>
<td>Electroplating (Ni, Sn-Pb)</td>
<td>Proprietary System</td>
</tr>
<tr>
<td>Bump Reflow</td>
<td>ATV SRO-704-R formic acid oven</td>
</tr>
<tr>
<td>Wafer Thinning</td>
<td>Strasbaugh 7AF Intelligent Grinder</td>
</tr>
<tr>
<td>Dicing Saw</td>
<td>Disco DFD651</td>
</tr>
<tr>
<td>Flip Chip Bonder</td>
<td>Suss MicroTec FC150</td>
</tr>
</tbody>
</table>
Photolithography Step for Bumping

Bump opening on mask overlaps passivation via. Overlap is determined by field metal underetching & alignment accuracy.

Thick photoresist
Opening in resist
Passivation via

Example: CERN ALICE1/LHCb readout.

Wafer Thinning

PROCESS STEPS

1. Front side protection/planarization: UV-curable back grinding tape laminated on bumped wafer.
2. Back grinding using diamond wheels with two different grit sizes (coarse + fine).
3. Defect layer left by mechanical grinding is removed by wet chemical etching or CMP (Chemical Mechanical Polishing).
4. Protective tape is UV-exposed and delaminated.

Strasbaugh 7AF Intelligent Grinder
NOTES

- Thickness down to 150 µm (200-mm/8” wafers).
- Total thickness variation (TTV) with protective tape < 5 µm over wafer.
- Post-grinding defect layer etching improves mechanical strength of die.

Strasbaugh 6DS-SP CMP System
Flip Chip Bonding

Flip chip assembly is done in a Class-10 clean room.

PROCESS STEPS

1. Preliminary alignment.
2. Detector and readout chips are adjusted exactly parallel using a laser autocollimator.
3. Lateral alignment (x,y, θ).
4. Pre-bonding compression of softened bumps.
5. Reflow bonding.

NOTES

- Chips are heated through custom SiC vacuum tools using infrared halogen lamps.
- Alignment accuracy: < 3 μm.
- Throughput: 3-4 bondings/hour.
Example: ALICE ‘Ladder’ Assembly

1. Readout

ALICE1/LHCb readout chip process:
- Readout wafer size 200 mm x 725 µm
- Bumping with eutectic solder: TiW/Cu/Ni(3 µm)/eut. Sn-Pb(13 µm)
- Bump pitch: x = 50 µm / y = 400 µm
- Wafer thinning to 150 µm
- Dicing to chip size of 13.7 mm x 15.9 mm
- Picking of KGD
- Number of bumps/chip: 8,192
Solder Bump on ALICE1/LHCb Readout Chip After Reflow

Target Solder Volume = 1.52 \times 10^{-14} \text{ m}^3
ALICE ‘Ladder’ Assembly [cont’d]

2. Detector

ALICE detector chip process
- Detector wafer size 125 mm x 200 μm
- Bump pad metallization:
  TiW/Cu/Ni(3 μm)/eut. Sn-Pb(3 μm)
- Dicing to chip size of 70.7 mm x 13.9 mm

Microscope image
3. Flip chip bonding

Hybridized ALICE assembly

- Five ALICE1/LHCb readout chips flip chip bonded on ALICE1 detector ladder chip
- Assembly reflow using formic acid oven
- Chip-to-substrate distance: 20 μm
- Total number of bumps/assembly: 40,960
Process Customization

- VTT’s ‘generic’ flip chip process has been customized to the wafers used by CERN, with consequent improvements in yield.
  - Field metal deposition on detector side: compatibility with polyimide passivation used.
  - Protection of detector wafer backside for bumping process.
  - Field metal etching: both sides.
  - Reflow on readout side.
  - Detector dicing process.
  - Flip chip bonding parameters.
  - 10-90 Sn-Pb solder process for LHCb assembly.
“VTT12” assembly (an early one, made in 2001) irradiated with a strontium source. Output scaled to “1” to show dead pixels. The number of dead pixels is 14 out of a total of 8,192.
ALICE1 Single: “VTT12”

“VTT12” assembly irradiated with a strontium source. Output scaled to max. “50” to show intensity of beam. The columnar imperfections are due to artefacts of the readout chip.
Yield Factors

- **Pre-bumping/assembly.** Foundry yield, particles generated in probing and handling (and history of wafers in general). Detector side: Defects in polyimide passivation.

- **Bumping/assembly.** Missing bumps, shorted bumps, high contact resistance (influenced by history of wafers), detector dicing, bonding yield.

- **Post-bumping/assembly.** Handling, correct test procedure, interpretation of test results.
Shortlist of Things…

• **Bumping layout design**
  - **Alignment targets** with known locations are required on wafers (and matching targets on masks).
  - **Three smooth areas of at least 50 μm in diameter** are needed on both detector and readout chips at the same mutually aligned locations near chip periphery for laser leveling in flip chip bonder.
  - Preferably single dicing lane in between chips, and no metal on dicing lanes (on either side of wafer). Avoid layouts which cannot be diced in a single run. **Kerf width** in dicing is non-zero!
  - Potential **stitching problem** with stepper-processed wafers (1:1 contact aligners used at VTT).
Shortlist of Things... [cont'd]

- **Readout & detector wafers**
  - Minimize handling of wafers outside clean room environment.
  - Probing marks may have an effect on bumping process.
  - **Whole wafers** preferred for bumping!
Future Trends

• Reliable flip chip bonding process with bump size of around 10 μm in diameter will be needed in near future.
• Use of non-Si detector materials gives rise to thermal mismatch in contrast to readout asic made of Si. Low melting point solder alloys needed to minimize thermal stress.
• Lead free solder bumps?
• For large area pixel detectors, bump bonding alignment and autocollimation accuracy needed is at the limit of existing tools.
Summary

• A brief overview of VTT’s bumping and flip chip assembly capabilities was presented.
• The hybridization of CERN’s ALICE detector was shown as an example.