Future trends in radiation hard electronics

F. Faccio
CERN, Geneva, Switzerland
Outline

• Radiation effects in CMOS technologies

• Deep submicron CMOS for radiation environments

• What is the future going to look like?
Summary of radiation effects

Total Ionizing Dose (TID)

Cumulative effects

Displacement damage

Permanent SEEs
SEL, SEGR?

Single Event Effects (SEE)

Static SEEs
SEU, SEFI
Digital ICs

Transient SEEs
Combinational logic
Operational amplifiers

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Total Ionizing Dose (TID)

Ionization in SiO$_2$
(charged hadrons, electrons, gammas, …)

↓

Creation of electron-hole pairs

↓

Buildup of charge/defects

↓

Device degradation
TID in CMOS devices

F.B. McLean et al., HDL-TR-2129, internal report, 1987

Trapped holes $\Rightarrow$ Vt shift, noise, leakage

Interface states $\Rightarrow$ Vt shift, mobility, transcond.

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Transistor level leakage

Parasitic MOS

Parasitic channel

Trapped positive charge

Field oxide

Bird’s beak

Source

Drain

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IC level leakage

SOLUTION: GUARD RINGS
Single Event Effects (SEE)

Very localized events (in time and space) induced by a single particle (whilst TID and displacement are gradual cumulative effects).

They can be:

- Transient $\Rightarrow$ spurious signals propagating in the circuit
- Static $\Rightarrow$ errors overwriting information stored by the circuit
- Permanent $\Rightarrow$ or “Hard Errors”, they are destructive events
Single Event Upset (SEU)

Along the ion track, e-h pairs are created. In presence of an electric field (depleted junction), the charge will flow and a current spike might be observed.

Example: SEU in a static RAM

L. Massengill, IEEE NSREC short course, 1993
SEU: which particles?

Heavy ions (space) => high dE/dx (LET, in MeV•cm²/mg)

Hadrons (LHC) => low dE/dx, but nuclear interactions
Single Event Latchup (SEL)

Electrical latchup might be initiated by electrical transients on input/output lines, elevated T or improper sequencing of power supply biases. These modes are normally addressed by the manufacturer.

Latchup can be initiated by ionizing particles (SEL)

SEGR in power MOSFETs

SEGR is caused by heavy-ion-induced localized dielectric breakdown of the gate oxide

‘Classical’ solution

Use a dedicated radiation-hard technology (TID, SEL)

Use dedicated libraries for SEU, and/or TMR, duplication, EDAC, …
Radiation effects and $t_{ox}$ scaling


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Standard and enclosed geometries (ELT)
Radiation tolerant approach: motivation

$$\Delta V_{th} \propto t_{ox}^{n} + \text{ELT's and guard rings} = \text{TID Radiation Tolerance}$$

Deep sub-\(\mu\)m means also:

- speed
- low power
- VLSI
- low cost
- high yield

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Density and speed

A & B : 0.6 \( \mu m \) standard
C & D : 0.25 \( \mu m \) rad-tol

Inverter with F.O. = 1

\[
\begin{array}{c|cc}
\text{Area} & 0.6 \mu m & 0.25 \mu m \\
\hline
\text{V}_{DD} [V] & 3.3 & 2 \\
\text{Delay [ps]} & 114 & 48 \\
\text{Pwr [\mu W/MHz]} & 1.34 & 0.14 \\
\text{Area [\mu m^2]} & 162 & 50 \\
\end{array}
\]
Total dose results up to 30 Mrad

Threshold voltage

Leakage current

Output conductance

Mobility degradation:
< 6% NMOS
< 2% PMOS

0.25 μm technology
N-channel noise spectrum

**Noise [V/Hz^{1/2}] vs Frequency [Hz]**

- **Prerad**
- **After 100 Mrad**
- **After Annealing**

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Single Event Latchup (SEL)

**NO latch-up observed up to 100 MeVcm$^2$mg$^{-1}$**

- SEL is also design-dependent
- The systematic use of guardrings is an effective tool against SEL
- In LHC, the maximum LET is lower than 50 MeVcm$^2$mg$^{-1}$
\[
\left(\frac{W}{L}\right)_{\text{eff}} = 4 \frac{2\alpha}{\ln \frac{d'}{d' - 2\alpha L_{\text{eff}}}} + 2K \frac{1 - \alpha}{1.13 \cdot \ln \frac{1}{\alpha}} + 3 \frac{d - d'}{L_{\text{eff}}}
\]
Technology scaling

Year

Transistors per chip
[Million]

On Chip Speed [GHz]

Min. Logic Supply Voltage [V]

Min. Gate Length / 100 [nm]

Semiconductor Industry Association

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Radiation effects and $t_{\text{ox}}$ scaling

Measured on VLSI tech.

$\Delta V_{\text{th}}/\text{Mrad(SiO}_2\text{)}$ [V/rad(SiO$_2$)]

- 1.6
- 1.2
- 0.8
- 0.5
- 0.5 - A
- 0.5 - B
- 0.35
- 0.25 - A
- 0.25 - B
- $t_{\text{ox}}^2$

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SEU and scaling

- $V_{DD}$ reduced
- Node C reduced
- New mechanisms for SEU

With the scaling the SEU problem worsens!

P.E. Dodd et al., IEEE TNS, Dec. 1996

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SEU and scaling

• All sources agree: DRAM sensitivity has been scaling down (cell area scaling has outpaced the decrease in stored charge).

• Picture somewhat less clear for SRAMs
• P.Hazuka et al (work funded by Intel) developed a model to predict SER scaling with Lg. The results suggest that the per-bit sensitivity decreases – at least – linearly with Lg

• Overall: FIT/MB decreases, but FIT/chip increases

• Not only Vdd and node capacitance have to be taken into account: sensitive area and charge collection efficiency are also important and change with technology generation!

• **SEU has to be tackled at system level!**
SEL and scaling

- Retrograde wells
- Thinner epitaxial layers (?)
- Trench isolation
- $V_{DD}$ reduced

All these issues help in preventing SEL, but they might not be always effective
SEGR and scaling

- Two research works presented at NSREC01
- They studied SEGR and RSB of thin oxides (down to 2nm) with Heavy Ions:
  - J. Conley et al. found RSB at LET=60MeVcm²mg⁻¹, and this might influence the lifetime of the devices.
  - L. Massengill et al.: “All of the samples reached ion-induced hard breakdown at applied voltages well above typical operating power supply voltages”
What about SOI?

• SEL: better than bulk
• SEU: better than bulk
• SEGR: same as bulk
• TID: due to the thick buried oxide, and to the technological solutions chosen for commercial-grade SOI, this will be the dominant radiation problem in a multi-Mrad environment!
Conclusion

• The market for dedicated radiation-hard processes has been constantly shrinking in the last decade, whilst the scaling down of VLSI technologies is proceeding at high pace

• Commercial-grade technologies do not show any stopper to their use in a multi-Mrad environment, but require:
  – Radiation-tolerant layout practices (ELTs, guardrings)
  – SEU to be addressed at global level