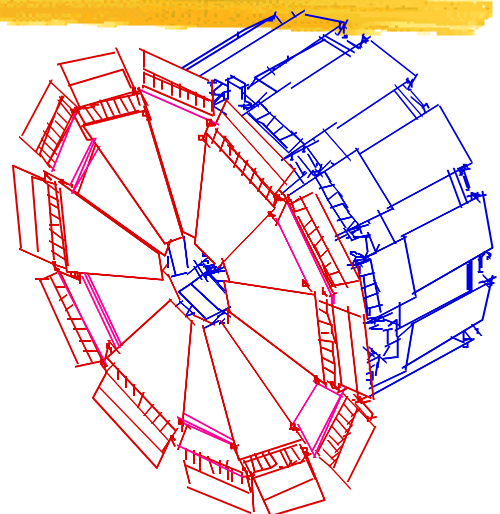
Quality assurance for the DØ silicon tracker



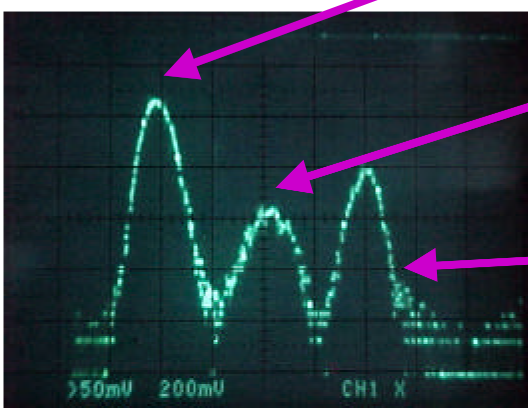
- Run2, DØ and the silicon tracker
- Quality assurance during production
  - sensors
  - chips/ flex circuits
  - ladders
  - system tests
- Concluding remarks

Frank Lehner
U of Zurich/ Fermilab
On behalf of the
DØ Collaboration

First $p\bar{p}$ collision at DØ
April 3, 2001

- Luminosity counters
  - timing:

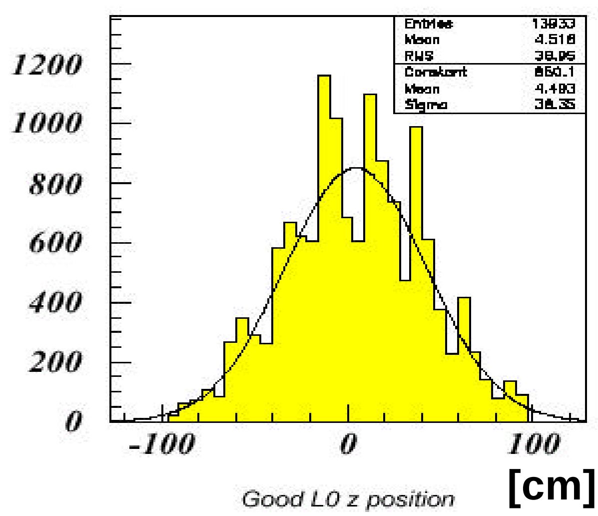
Antiproton halo



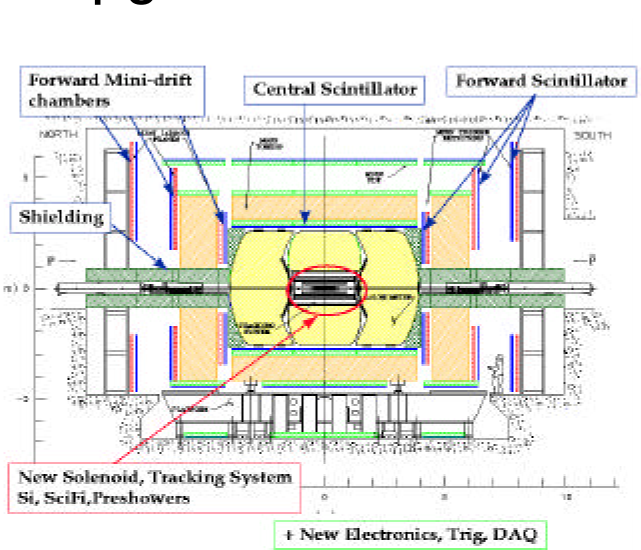
Luminosity
(coincidence)
~5 × 10^{27} cm^{-2} sec^{-1}

Proton halo

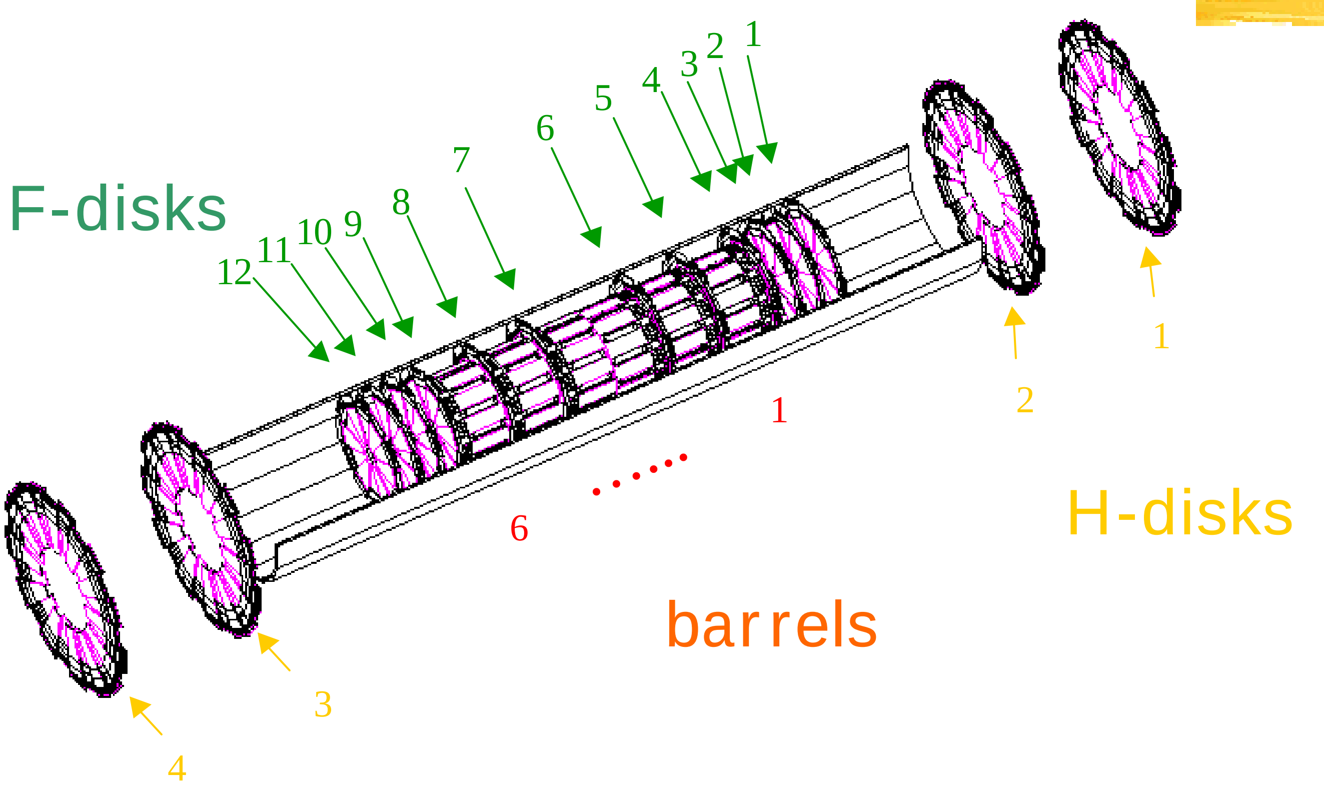
Vertex distribution along z of min bias events:



Run2 has started with an upgraded detector:



The DØ silicon tracker



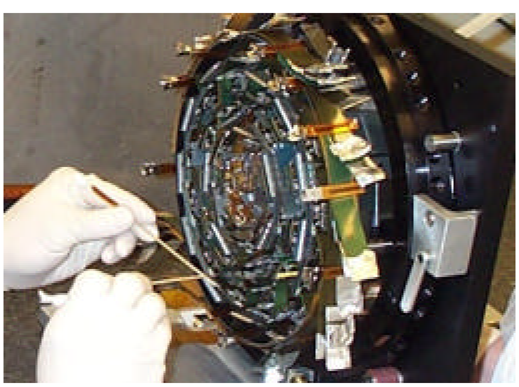
- 6 barrels, 4 layers of silicon, interspersed F-disks, design driven by large interaction region (σ=25cm) w/ good acceptance for high p_t tracks
- large area external H-disks for forward tracking $2<|\eta|<3$
- Detector & inboard electronics moderately rad-hard (4MRad)

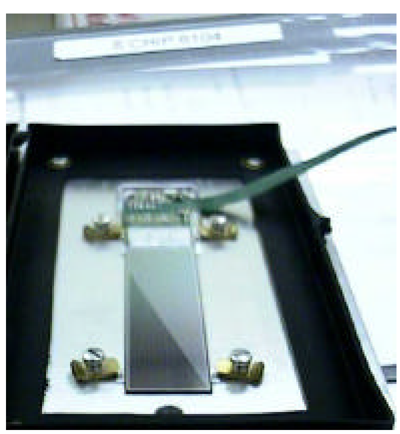
	Barrels	F-Disks	H-Disks
Channels	387120	258048	147456
Modules	432	144	96
Inner R	2.7 cm	2.6 cm	9.5 cm
Outer R	9.4 cm	10.5 cm	26 cm

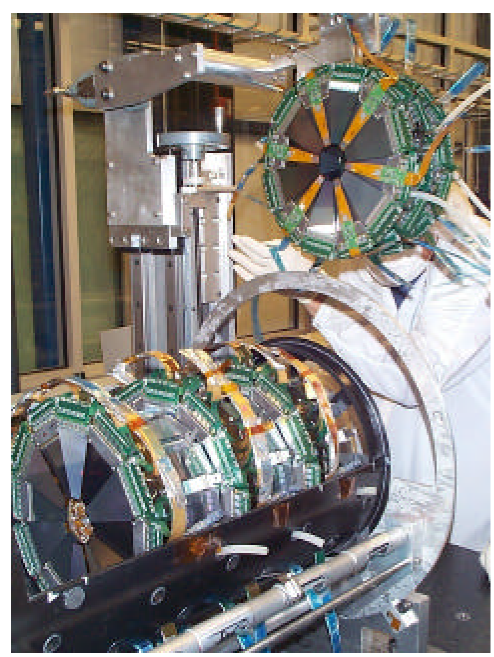
total 793,000 channels !!

The DØ silicon tracker

- silicon tracker has been built within 18 months:
  - formidable production job
    - ✓ tested and assembled ~1400 silicon pieces with a total wafer area of 3.2m^2 to build more than 800 ladders
    - ✓ debugged & repaired ladders
    - ✓ placed ladders into barrels and wedges onto disks
    - ✓ assembled barrels/disks to two half detectors
    - ✓ inserted two halves into DØ

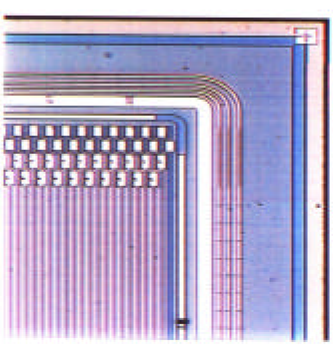


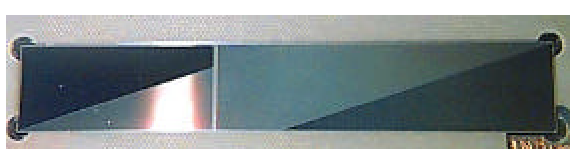


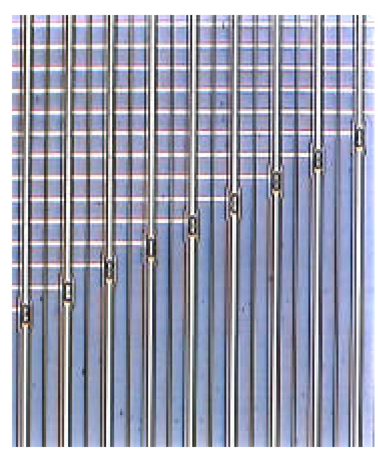


Sensor types

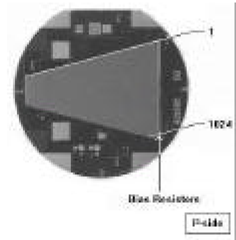
- 5 different sensor types:
  - **Barrels:**
    - ✓ double sided with 2º-stereo strips, pitch 50µm on p-side, 62.5µm on n-side, AC-coupled, polysilicon bias on 4”-wafers
    - ✓ double sided with 90º-stereo strips and double metal layer, pitch 50µm on p-side and 153µm on n-side, AC-coupled, polysilicon bias on 6”-wafers
    - ✓ single sided with 50µm pitch, AC-coupled and polysilicon on 4”-wafers
  - **Disks:**
    - ✓ double sided wedges with ±15° variable strip length, AC-coupled and polysilicon on 4”-wafers
    - ✓ single sided wedges glued back to back with ±7.5º
  - Main vendors: Micron/UK, ELMA and Eurisys
- Total amount: ~1400 sensors







Sensor specifications



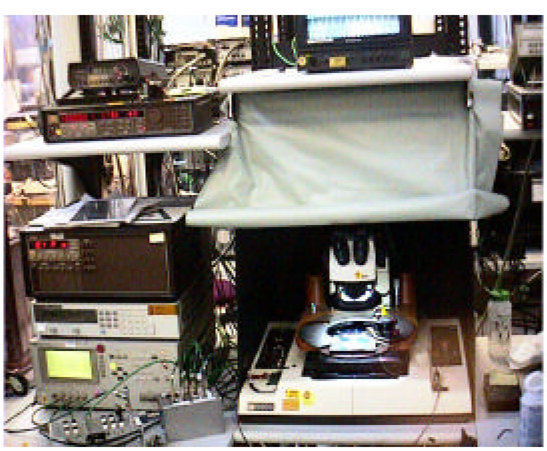
- wafer thickness 300 ± 20 μm
- leakage current <0.5μA/cm² @ $2U_{depl}$
- breakdown voltage >100V
- depletion voltage $20<U_{depl}<60V$
- bias resistor R_{bias}
  - $1<R_{bias}<10M\Omega$
  - uniformity better than ±25%
- interstrip resistance >100MΩ
- coupling capacitors
  - ~15pF/cm
  - channels outside ±15% fail
  - coupling capacitor breakdown 100V for both sides n/p
- interstrip capacitance <1.5pF/cm
- bad channels (short, open, pinhole)
  - generally 2%
  - 4% in case of n-side with double-metal layer
- specs lowered during sensor prod. in order to achieve higher deliv. rate

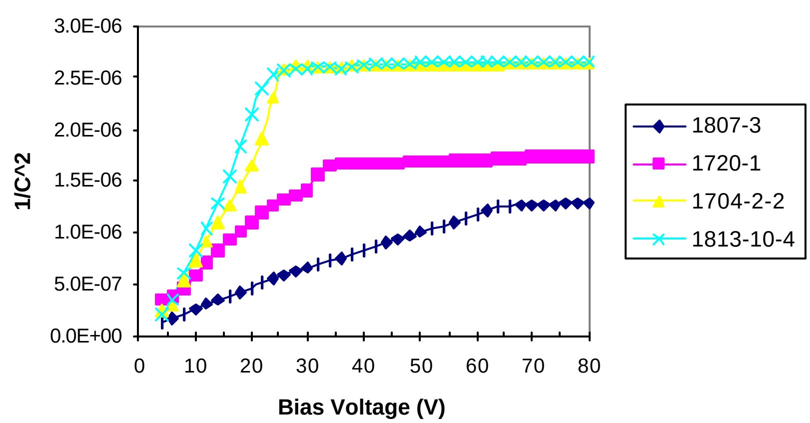
Sensor quality assurance

- originally planned:
  - have probe testing of production sensors at vendor and to test only small samples at Fermilab/Universities as cross check
- did not work as anticipated:
  - discrepancies of measurements, reliability of testing at vendor, short manpower at vendor, low delivery rates with double sided detectors
- decided to send own probe equipment and manpower to main vendor:
  - had for more than 20 months own technician(s)+equipment locally present to test F-disks and 2º-stereo sensors
  - set up 2 automatic probe station at vendor
  - local presence improved a lot
    - ✓ reliable acceptance testing
    - ✓ immediate feedback to process engineer
    - ✓ overall increase of delivery rates
  - due to its complexity the double-sided double-metal sensors were locally tested by Micron personnel and retested at Fermilab

Sensor probing

- measured on manual/automatic probe station on each sensor:
  - C-V => U_{depl}
  - I-V => I_{bias} & I_{guard} & $U_{breakdown}$
  - AC cap values for all channels
  - test caps for breakdown by ramping up voltage across cap of up to 100V => search for pinholes
  - bias/interstrip resistors
  - strip currents measured on samples
- results stored in traveler system and data base => information used for production (e.g. bond skipping)

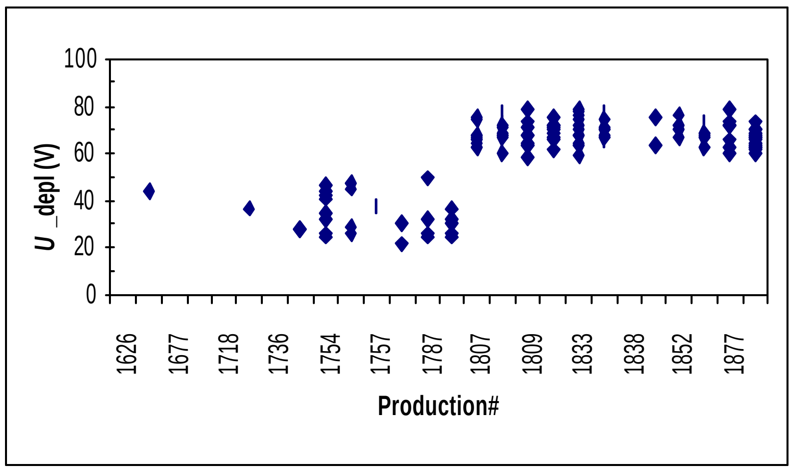




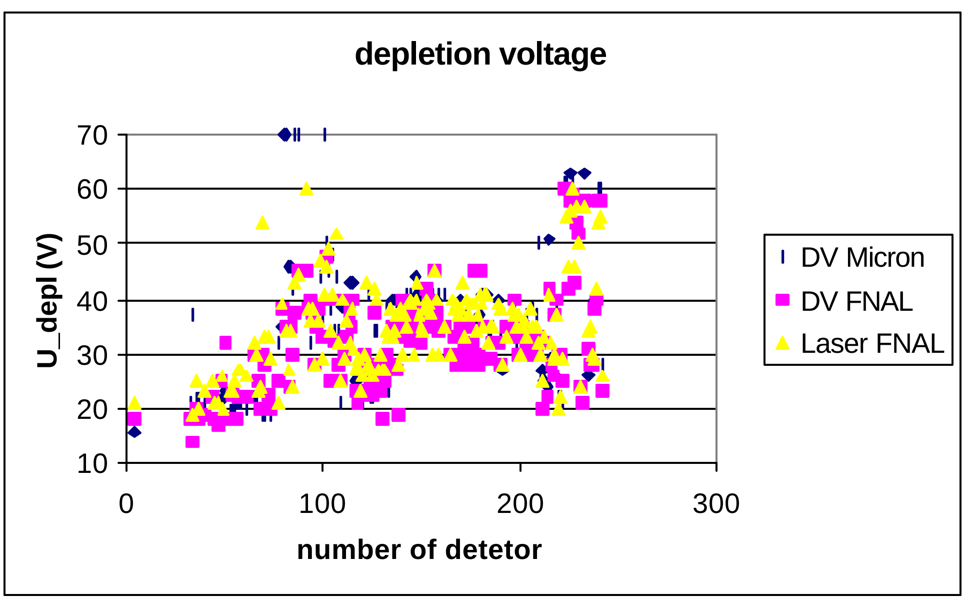
Evolution of depletion voltage

- wafer resistivity changes during production
- for a just-in-time production large fluctuations in characteristic depletion voltage made barrel assembly difficult

F-disk: also crystal orientation change (111)->(100)

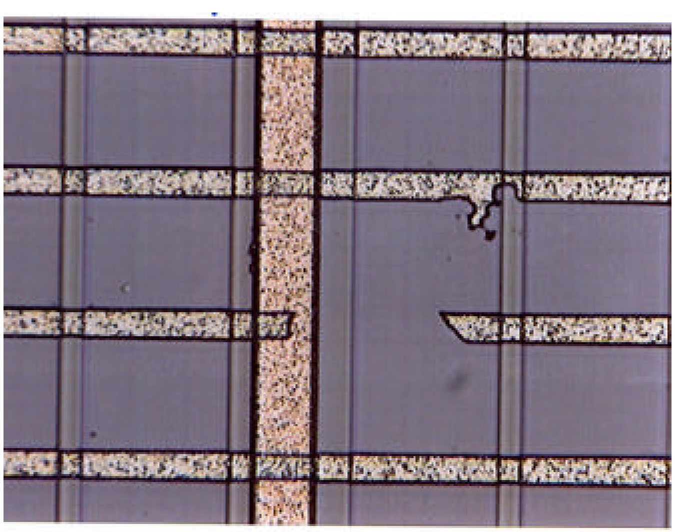


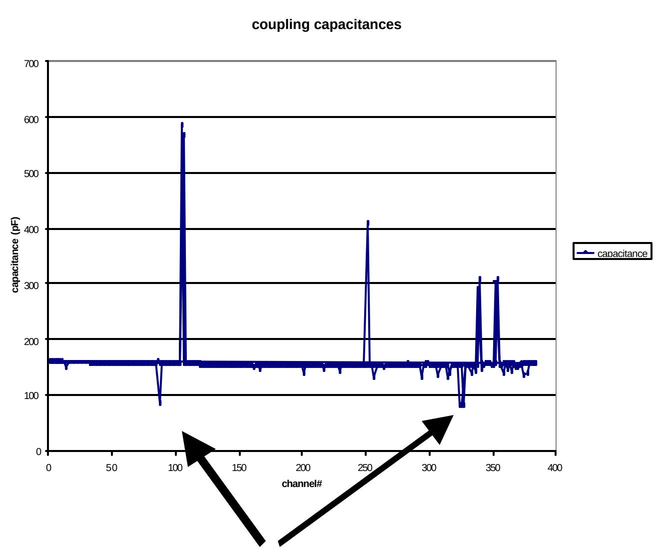
90º sensors: large fluctuations in U_{depl} at end of production



Sensor problems

- each of our different sensor type had its own maladies ...
- 90º double-sided double-metal:
  - initially serious problems with fragile double metal layer
  - could be cured by increasing metal thickness

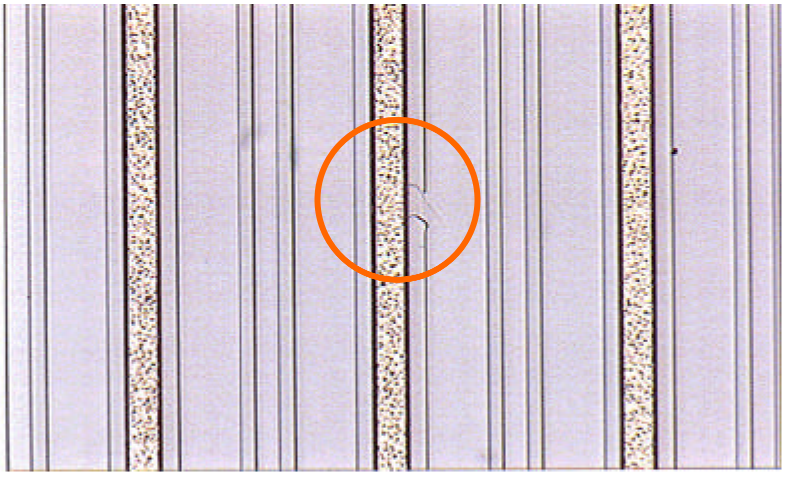




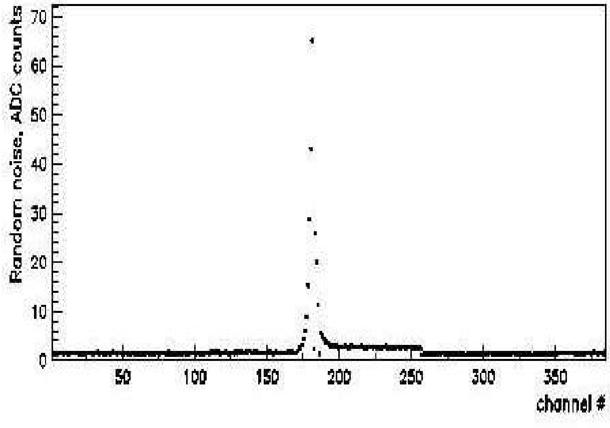
Measure ½ of capacitance

p-stop isolation problem

- p-stops on n+ to provide strip isolation
- 90º sensors have combined p-stops (1 individual + 1 common frame)
- observed on some ladders high excess noise caused by a single strip
- strips had defects in individual p-implants
- careful visual scans did not catch this entirely, but single strip leakage measurements
- yield reduced considerably to ~35%
- problem could be partially traced back to mask defects

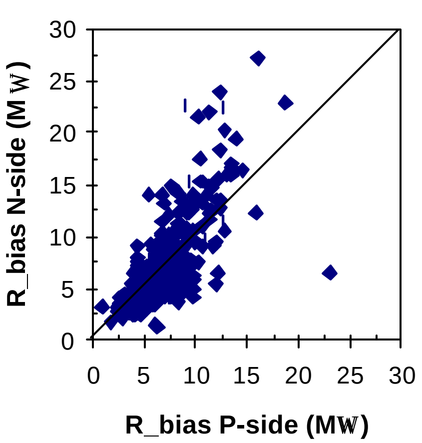


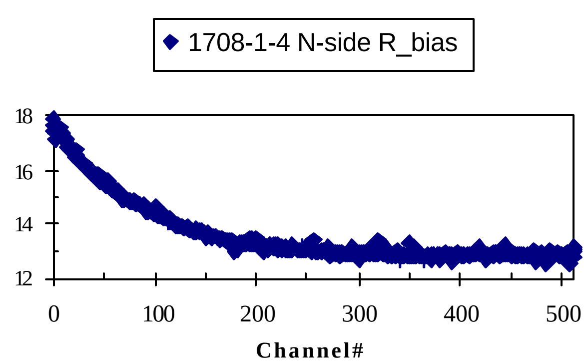
noise of strips



Sensor problems

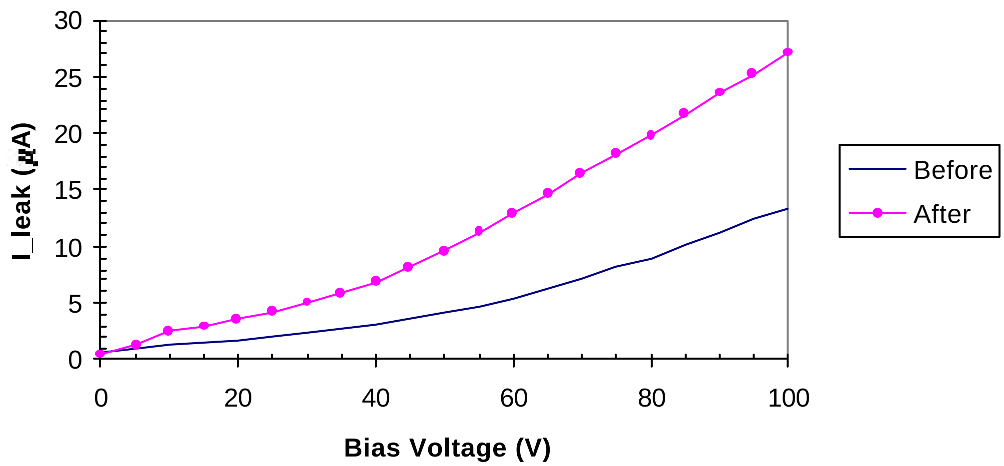
- 2º stereo sensors:
  - high values (>10 MΩ) for the bias resistors R_{bias}
    - ✓ resulted in significant worsening of testing yield for some period of time
    - ✓ protective PECVD layer above polysilicon was missing, plasma etching caused high R_{bias} values
  - partially large inhomogeneity (50%) across strips for bias resistor R_{bias}
    - ✓ strips received non-uniform implanting
    - ✓ solved by outsourcing ion implanting





Current instabilities

- leakage current changes after probing p-side:
  - significant increase in current after probing appeared during several months and was a temporary phenomena
  - fortunately most of affected sensors went back to normal currents after several days/week
  - although investigated we could not clarify this effect nor make any conclusive link to processing

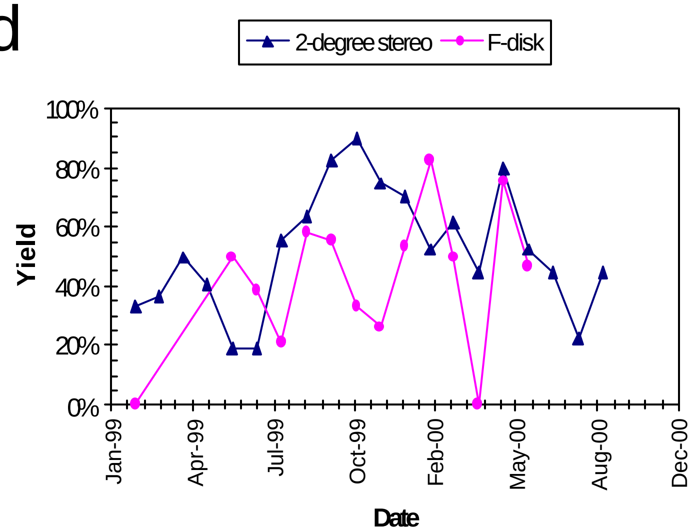


low interstrip resistance

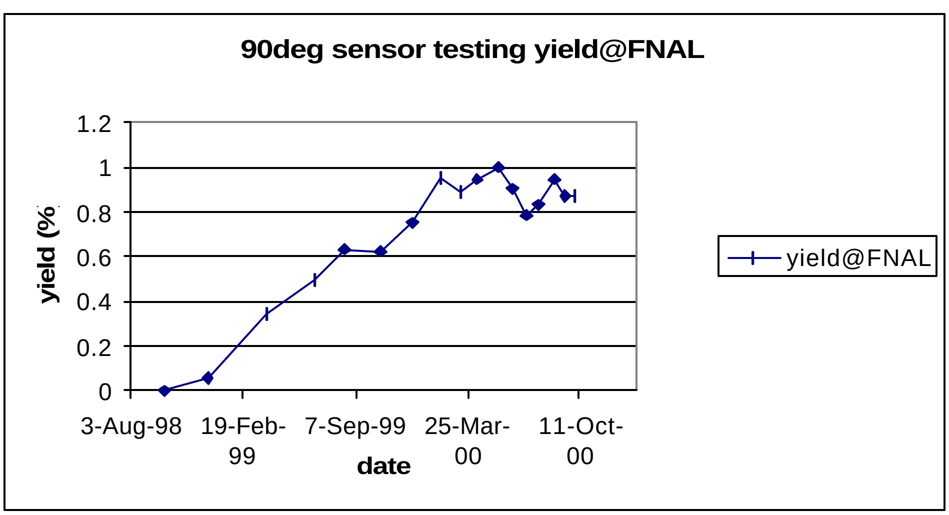
- early sensors in 1998 had low interstrip resistances of few kΩ on p-side
  - probably caused by contaminations in the Nitrogen purge gas
  - mobile charge in oxide => loss of strip isolation ?
  - problem disappeared after additional purge gas was exchanged and additional cleaning/rinsing steps have been introduced
- this and the previous phenomena indicate that the oxide quality plays an important role and should be part of the QA process
  - we did not fully exploit measurement capabilities on teststructures e.g.
    - ✓ measure flatband shifts regularly on MOS structures
    - ✓ measure mobile oxide charge (Na+) at elevated temperatures ...

Overall acceptance yield

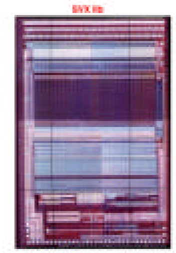
- (our) acceptance yield of F-disk and 2º-sensors varied strongly over time, in average ~40-50%



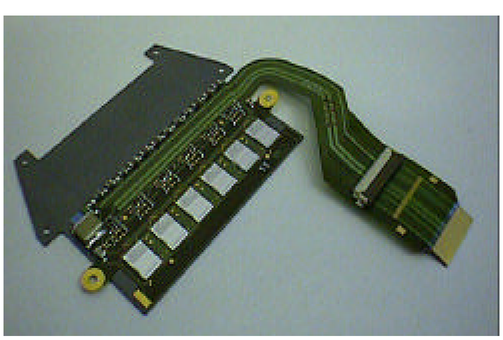
- our testing yield at Fermilab of 90º-sensors improved steadily (note: this yield does not include Micron production yield: ~40%)

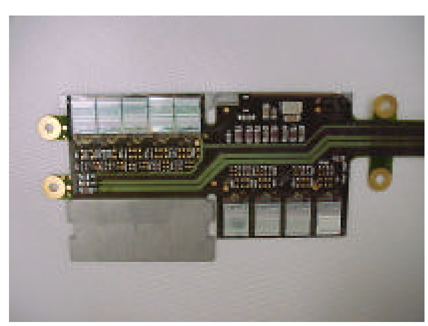


Chip/HDI



- use SVXII chip (1.2μm CMOS)
  - preamplifier, 32-cell pipeline, 8 bit ADC and sparse readout
  - chips developed at FNAL/LBL and tested
- high density interconnect (HDI)
  - Kapton based flex circuit
  - our geometry required 9 different types !
  - fabrication/testing:
    - ✓ bare HDIs visual inspected and traces tested for shorts
    - ✓ laminated to Be-substrate and components mounted
    - ✓ HDI package tested and burnt-in





System test

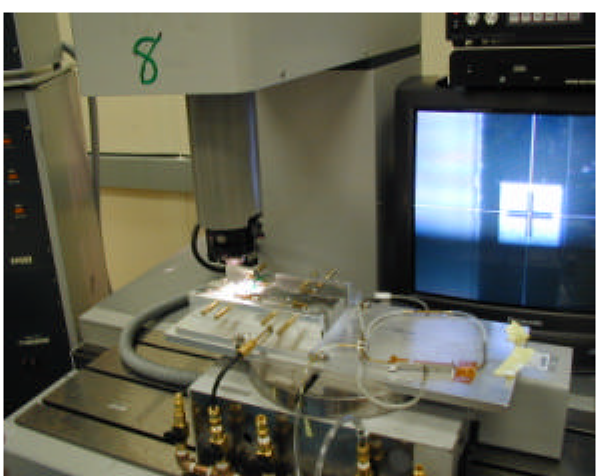
- Set up and perform from early on a small scale system test
  - test the full R/O chain
  - detailed noise/timing studies of SVX and R/O boards
  - electronics integration
  - understanding of cabling, electronics and system problems
  - achieved tiny error rate of less than 10^{-14}
  - test turned to a real 10% system test when a full barrel/disk module was read out

system test was unbelievable crucial in getting the detector to work ...

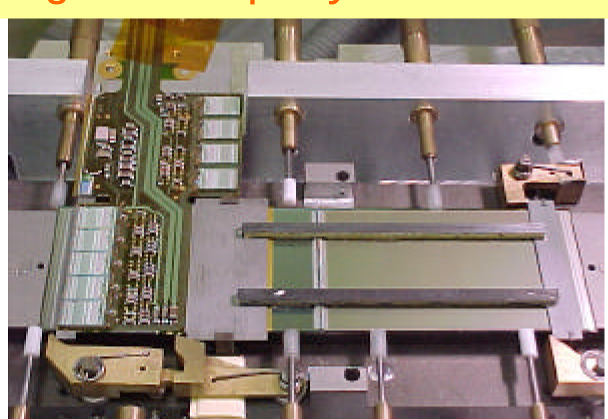
QA during ladder construction

- laminated Be substrate on HDI glued on one side of silicon (HDI then wrapped over and glued to other side)
  - mechanical position of Be piece(s) w.r.t silicon targets crucial since it defines ladder position in barrel
  - assembly done under CMM control
  - remeasured several times during ladder construction and before insertion into barrel
  - achieved ladder accuracy of ~5μm in-plane
  - ladder flatness (warps) ~30-50μm

align sensors with CMM on fixtures

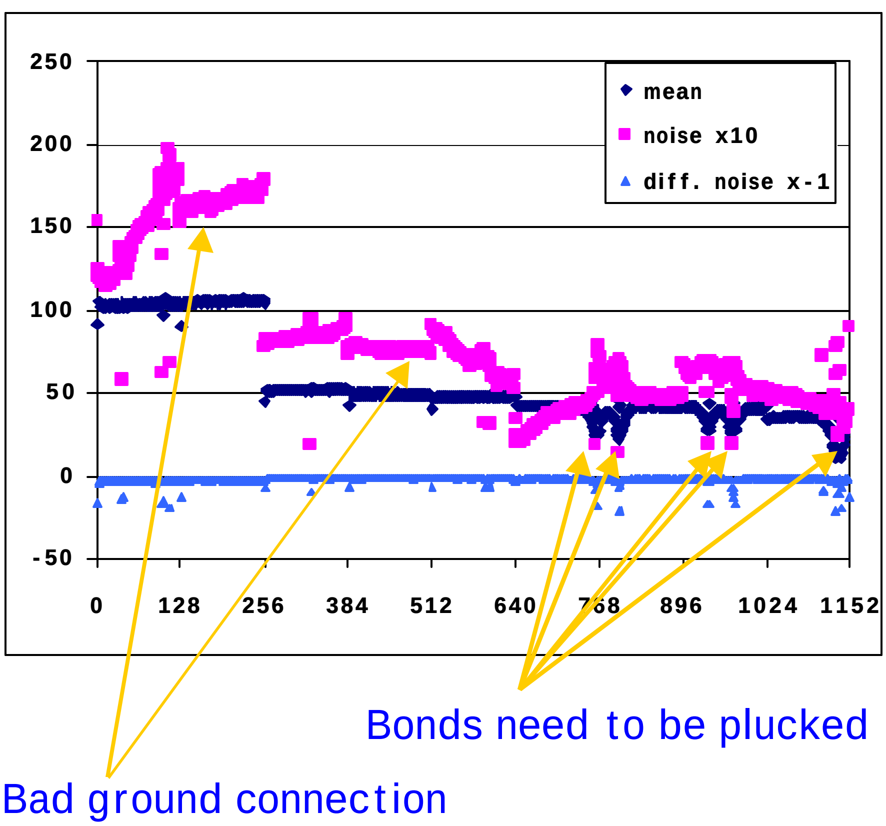


Check position of Be notches and glue w/ epoxy on Silicon



QA on ladders: debug/repair

- immediately after assembly ladders were subject to a debugging/repair phase:
  - thorough visual inspection
  - test of grounding of Be substrate
    - ✓ causes bad pedestal structures, common mode shift => indium solder/silver epoxy
  - look for remaining shorted pinholes by slowly applying ±HV on n/p-side
    - ✓ pull wirebonds

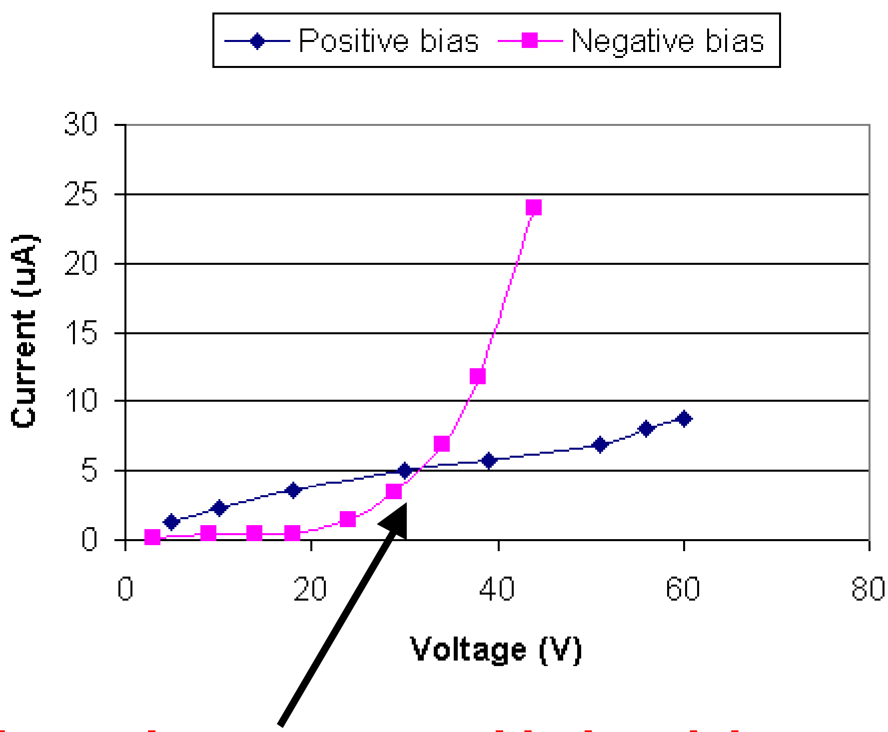


QA on ladders: debug/repair

- however: had some damage during our complex assembly of ladders, repairs were necessary
  - ✓~20% of ladders did not download and/or had a chip/circuit problem
  - ✓missing/touching control bonds
  - ✓damaged flex circuit pigtail
  - ✓chips could be replaced on ladder
- tools available
  - ✓dedicated debug/repair team (physicists + technicians)
  - ✓stand alone DAQ test stands
  - ✓probe stations
  - ✓logic analyzer
- overall yield of repair work was ~85%

QA on ladders: HV

- ±HV curves were taken to determine leakage currents and micro discharge limit for p-side
  - currents for ±HV for double sided detectors quite different
  - breakdown on p-side appears earlier if AC-capacitor is held on GND



determine V_{-max} p-side breakdown voltage

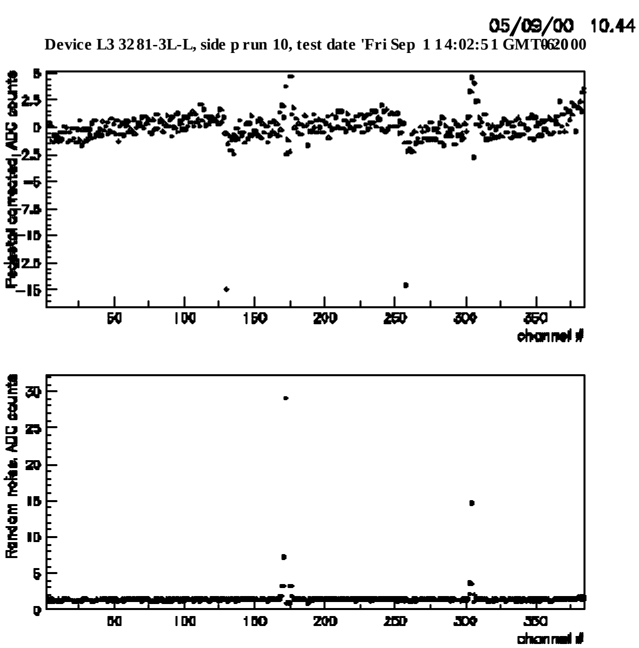
important parameter for split bias operation

p-side breakdown/micro discharge

- With n side at ground and p side on negative potential we observed a burst-like noise, if the capacitors are ground. Observation is consistent with micro discharges at the edge of strips (as seen by KEK group KEK 93-129).
- steep increase in strip current and earlier junction breakdown
- effect correlates with misalignment of Al-strips and implant
- effect caused by field distortions and charge accumulation near the p-implant when p-side capacitor is grounded. Effect does not appear on the n+ strips
- we should expect that after irradiation and type inversion from n to p silicon the effect should be mitigated on the p side and moves to the n- side, where the junction is **=> later**

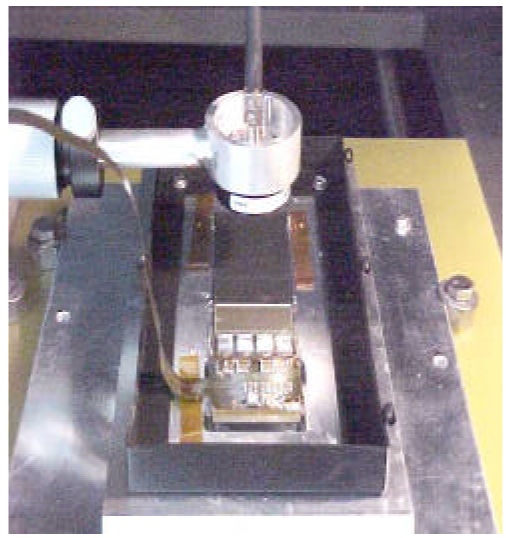
Ladder QA: burn-in

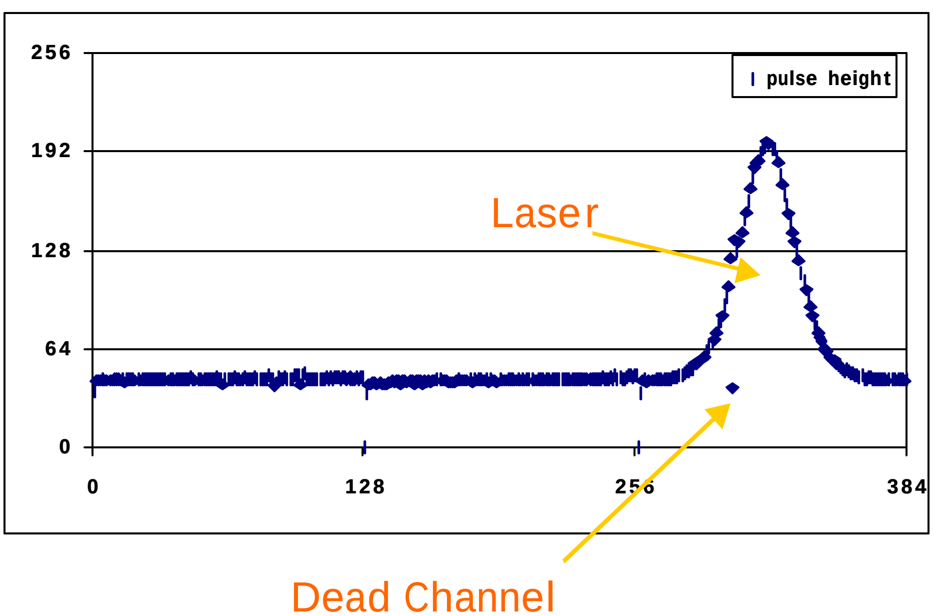
- after debugging/repair ladders were subject to a burn-in run of up to 72h
  - data integrity check, multiple downloads
  - pedestals/noise
  - gain per channel
  - test sparse readout
  - long term HV voltage operation (cooled) => currents



Ladder QA: laser test

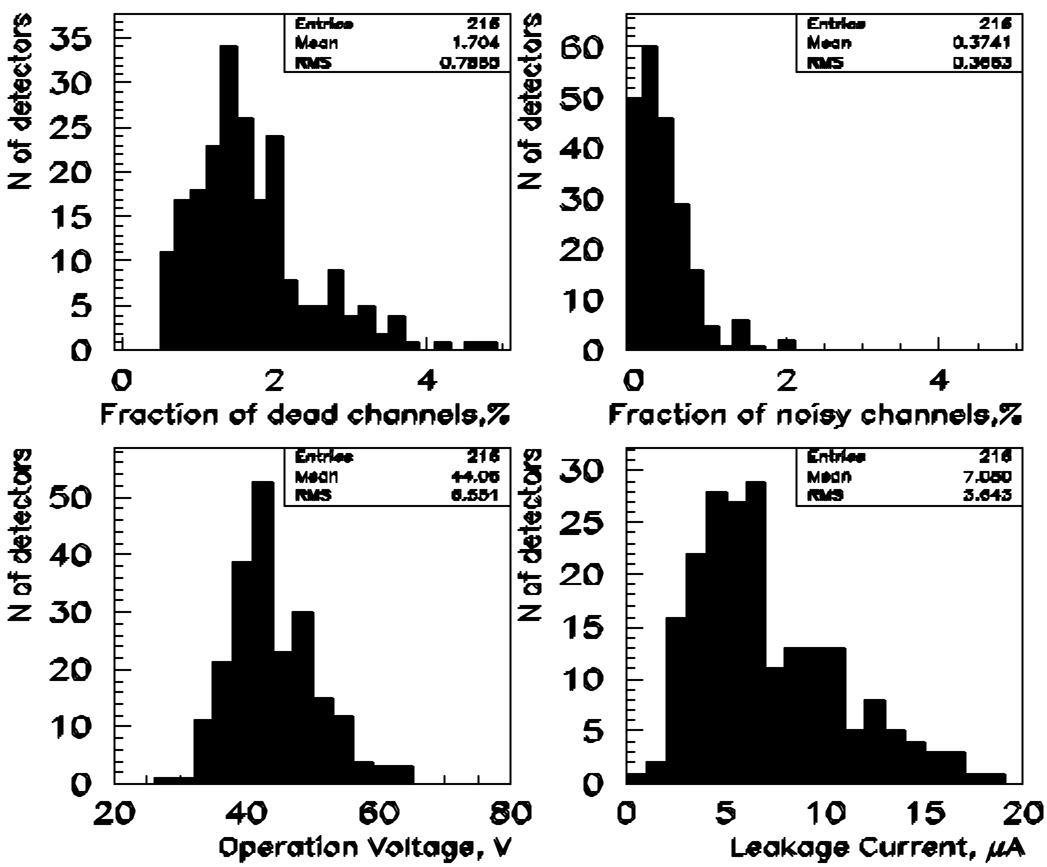
- test ladder after burn-in on laser stand(s)
  - 1064 nm laser light
  - traverses 300µm Si
- goals:
  - measure charge collection efficiency and depletion voltage
  - complete scan across strip
    - ✓ check homogeneity
    - ✓ check dead channels





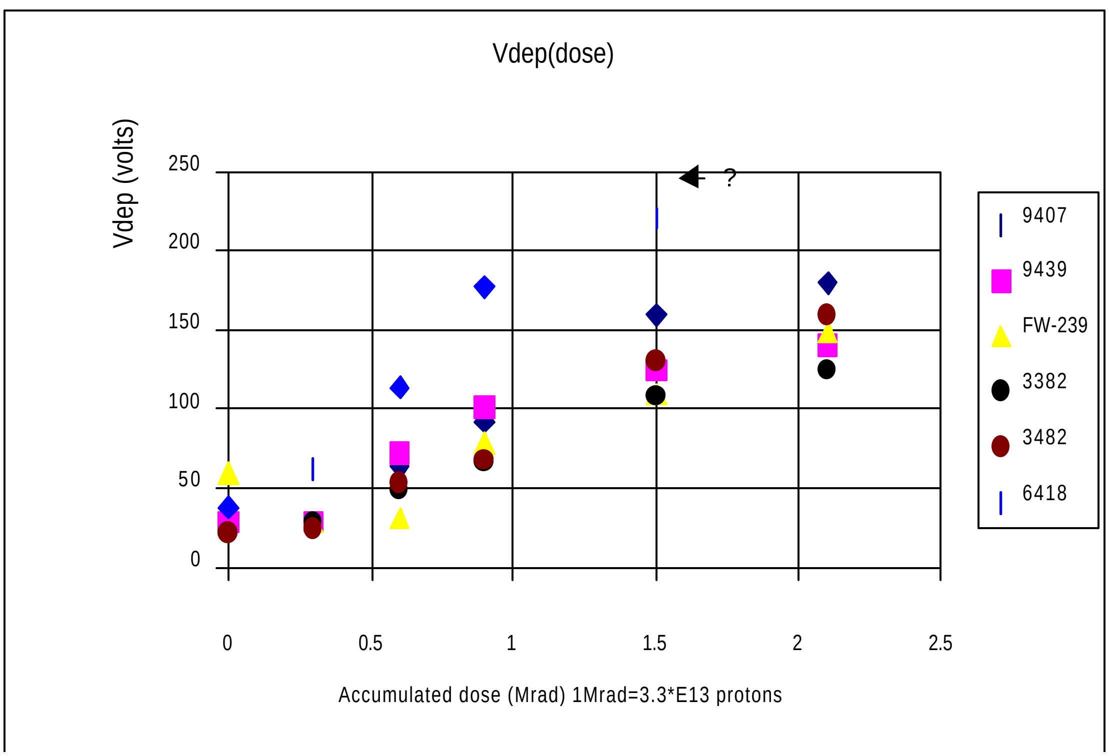
Ladder QA: grading

- grading system for ladders:
  - mechanical accuracy
  - # of noisy strips from burn-in
  - # of dead channels from laser
  - leakage current & V^{-}_{max}
    - ✓ grade A: less than 2.6% dead+noisy (10 per 3x128=384 strips channels
    - ✓ grade B: less than 5.2% dead+noisy channels



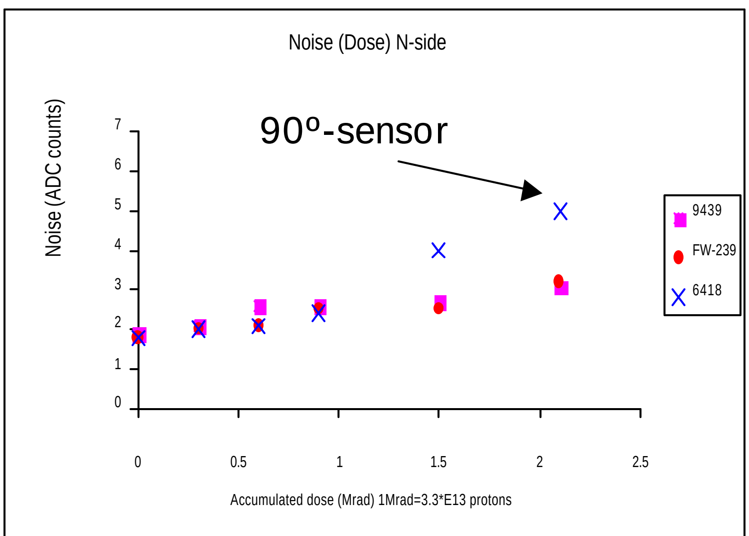
Radiation test

- carried out a new irradiation test with 8GeV p at Fermilab booster in Feb/Mar 2001
- irradiated ladders up to 2.1 MRad in 5 steps (~min 4 years RunIIa in inner layer)
- depletion voltage of most ladder types agree, except 90º-sensor ladder (double-metal) ... unclear ??

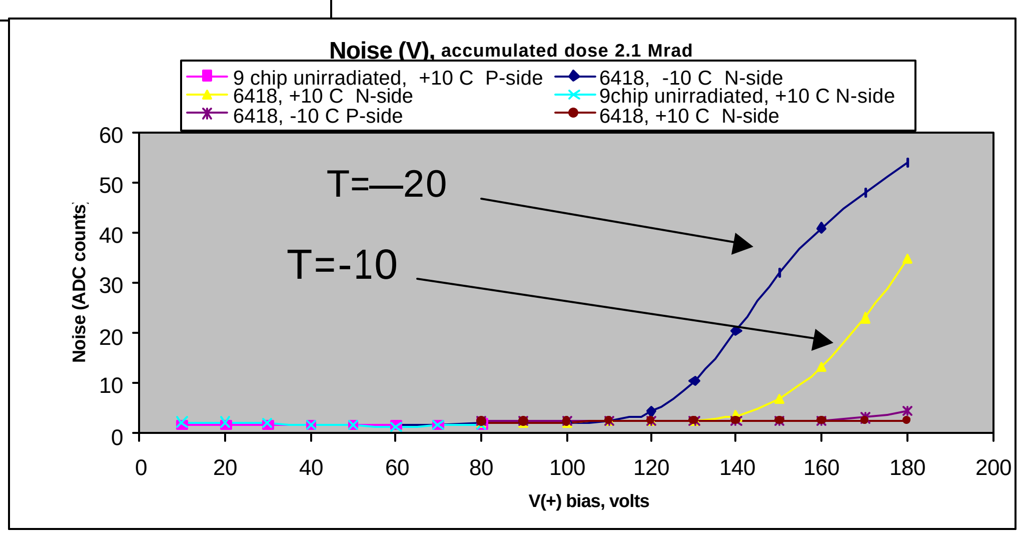


Radiation test

- also stronger increase in average noise on n-side for double-metal detector after irradiation
- observe temperature dependence of n-side noise:
  - the lower the Temperature, the earlier the noise occurs
  - mobility changes $\mu \sim T^{-2.3}$ => earlier junction breakdown



p-side noise (not shown) was immune against this effect. A hint that micro discharge has moved from P-side to n-side ??



Conclusions

- DØ silicon tracker has been built and is working (first tracks seen)
- production was a huge effort of many people, although only 3.2m^2 silicon area
- had tight QA measures at different stages of the fabrication process in place
  - sensors: thorough testing, quick feedback to vendor and local presence turned out to be crucial
  - ladders: multi-layer quality control (debug, burn-in, laser) with dedicated repair/debug teams and clear procedures was important
  - system test from early on helped us enormously
- however: much bigger logistical enterprise than originally anticipated:
  - too many detector types with too many single components with too many different vendors with too many delivery problems
- double-sided detectors may not be worth it: only moderately radiation hard